THÈSE

En vue de l'obtention du

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Mention : Génie Électrique

par

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« Optimization of DC/DC converters for embedded systems including dynamic constraints»

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Résumé en Français

En raison de la pénurie progressive de combustibles fossiles et de l'urgence environnementale, des accords internationaux ont été conclus pour contenir la croissance de la température moyenne mondiale à long terme. Les directives introduites visent à faire converger les flux financiers vers un développement économique respectueux de l'environnement et à orienter les efforts de la communauté industrielle vers une réduction des émissions des gaz à effet de serre, en particulier dans le secteur des transports, dont le taux d'augmentation de la consommation d'énergie (ainsi que des émissions de gaz à effet de serre) est le plus élevé au cours des dernières décennies.

L'industrie aéronautique et automobile privilégie des solutions plus efficaces et plus autonomes, ce qui a conduit à une électrification considérable des systèmes de conversion d'énergie à bord. Le marché des véhicules électriques ou hybrides électriques est en croissance constante. L'échange d'énergie entre les unités de stockage, le système d'actionnement du groupe motopropulseur, le moteur/générateur à combustion interne et les nombreuses charges est assuré par un réseau DC, et chaque source/charge nécessite l'insertion d'un convertisseur d'interface spécifique. En même temps, dans le réseau électrique du réseau d'avions modernes (More Electrical Aircraft, MEA), plusieurs unités mécaniques ont été remplacées par des homologues électriques, au profit de l'efficacité et du poids du système global.

Pour alimenter les différentes charges de puissance à bord, les unités d'électronique de puissance sont constituées de convertisseurs de puissance à découpage, dont le fonctionnement s'effectue par la commutation des transistors à semi-conducteurs. L'évolution des convertisseurs de puissance s'améliore en même temps que les progrès technologiques des dispositifs à semi-conducteurs. Comme expliqué dans le premier chapitre, les dispositifs à base de silicium domine le marché depuis les trois dernières décennies. Pour des applications d'une centaine de kW, le transistor bipolaire IGBT a été le dispositif le plus utilisé en raison de ses calibres de courant et de tension élevés (par rapport aux dispositifs unipolaires MOSFET). Néanmoins, en raison de la nature bipolaire de la structure IGBT, la fréquence de commutation du convertisseur de puissance, lorsque ce dispositif est utilisé, est limitée par les temps de commutation du dispositif. D'autre part, la recherche sur les matériaux semi-conducteurs à grand gap (WBG, wide band-gap) a conduit à l'introduction de nouveaux dispositifs à hautes performances suffisamment matures pour être proposés sur le marché. Les caractéristiques des matériaux WBG comme le carbure de silicium ou le nitrure de gallium permettent de construire des dispositifs unipolaires, comme le transistor à effet de champ métal-oxyde-semiconductor (MOSFET), avec les mêmes calibres de courant et de tension des IGBT du commerce, une température de fonctionnement plus élevée, des pertes de conduction plus faibles et des temps de commutation plus rapides. La possibilité d'augmenter sensiblement la fréquence de commutation tout en maintenant les pertes de puissance à un faible niveau permet d'améliorer globalement le système de conversion en termes d'efficacité et de taille des éléments passifs et du système de refroidissement. La diffusion de ces dispositifs offre des possibilités évidentes pour considérablement améliorer les systèmes électroniques de puissance de conversion.

Compte tenu de ces critères, cette étude a pour objectif le développement d'une procédure de dimensionnement optimale d'un convertisseur dans un réseau embarqué. Le convertisseur a été conçu spécifiquement pour une structure d'alimentation d'un actionneur. Afin d'assurer la bonne interaction entre la charge (onduleur DC/AC et moteur) et le micro-réseau de bord, le dimensionnement doit prendre en compte la stabilité et le comportement dynamique du convertisseur lors d'une éventuelle variation du point de fonctionnement, donc sa stratégie de contrôle.

Le réseau de distribution d'énergie électrique à bord d'un avion moderne est composé d'un bus de tension alternative et d'un bus de tension continue alimenté par le réseau alternatif par l'intermédiaire d'unités de redressement, comme montré en Figure 1.

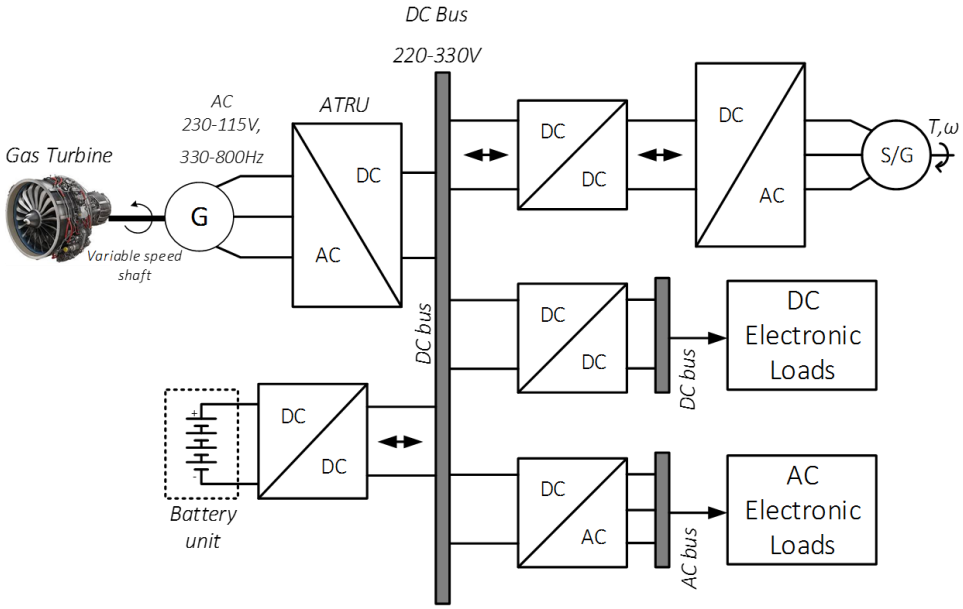


Figure 1 Exemple de micro-réseau DC embarqué dans un MEA.

Dans le cas spécifique des avions plus électriques, la variation la plus remarquable est l'absence de l'unité de boîte de vitesse (internal drive generator, IDG) pour la génération de l'énergie électrique AC à fréquence et à amplitude de tension fixes à partir de la turbine à gaz. L'amplitude et la fréquence de la tension alternative générée par la turbine sont variables, ce qui entraîne une modification de la tension du bus continu générée par un redresseur. Ensuite, les charges électriques et mécaniques sont alimentées par des convertisseurs DC/DC ou DC/AC (selon la charge) connectés au bus DC de distribution pour assurer une tension stable. Dans ce contexte, l'efficacité, la taille et le niveau d'intégration de la conversion électronique de puissance constituent les principales contraintes. Pour une application de groupe motopropulseur embarqué, l'étage d'électronique de puissance est souvent composé d'un simple onduleur connecté au bus DC par un filtre d'entrée (Figure 2(a)).

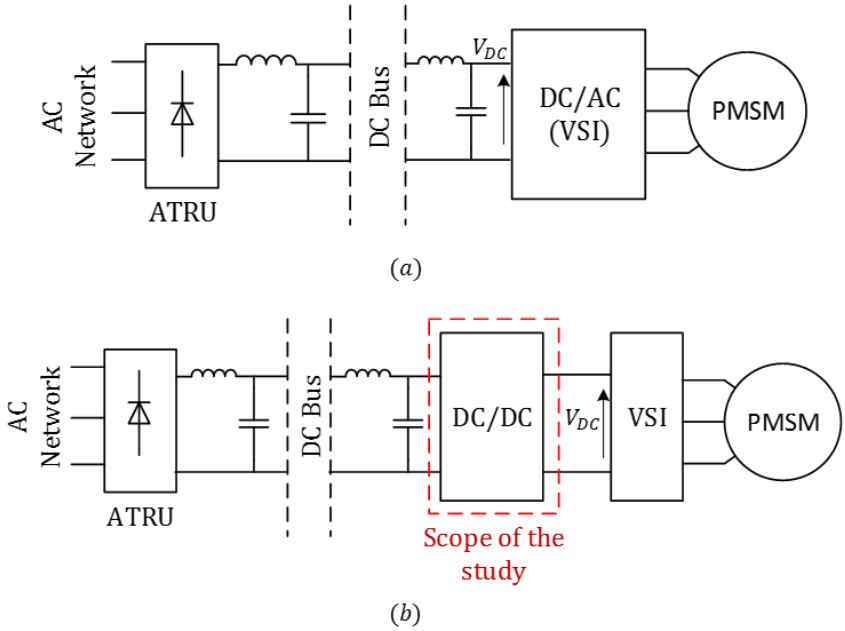


Figure 2 Chaîne de conversion classique (a) pour l'alimentation d'un moteur et avec un convertisseur DC/DC entre le bus DC et l'onduleur (b).

Comme expliqué dans le chapitre 2, une alternative intéressante consiste à insérer un convertisseur DC/DC entre le filtre et l'onduleur (Figure 2(b)). Cette solution permet d'immuniser l'onduleur contre les perturbations de tension sur le bus DC, en particulier dans le cas d'un réseau électrique dans un avion moderne. En effet, si la chaîne d'entraînement est uniquement composée de l'onduleur et du filtre d'entrée, les enroulements du stator du moteur doivent être conçus pour fonctionner de manière à assurer la contrôlabilité du couple moteur pour toute la plage de variation de la valeur de tension du bus DC, ce qui entraîne une augmentation des pertes de puissance dans l'onduleur et un surdimensionnement conséquent de ses composants actifs et de son unité de refroidissement. Le convertisseur DC/DC offre la possibilité d'optimiser l'efficacité de la chaîne d'actionnement dans toute la gamme de vitesse de fonctionnement.

En outre, un modulation d'amplitude (pulse amplitude modulation, PAM) pour la génération de signaux de commande peut être mis en œuvre, ce qui permet de réduire le nombre de commutations des dispositifs d'inversion pendant la période mécanique de la charge AC, dans ce cas un moteur synchrone à aimants permanents (PMSM), et diminue la distorsion de l'ondulation du courant dans les enroulements du moteur, ce qui est nuisible pour le moteur lui-même et pour le contrôle du couple. Les architectures de convertisseurs DC/DC les plus classiques ont été présentées pour la tâche envisagée. Selon le profil de la mission, il pourrait être plus avantageux d'utiliser un convertisseur élévateur pour une application à grande vitesse, ou un convertisseur élévateur/abaisseur pour une application à large gamme de vitesse.

Le chapitre 2 présente les topologies de convertisseurs DC/DC les plus courantes pour ce type d'application. Pour le cas spécifique de la chaine d'entrainement d'un actionneur démarreur (starter), une topologie originale de type "step-up/down" est présentée et analysée.

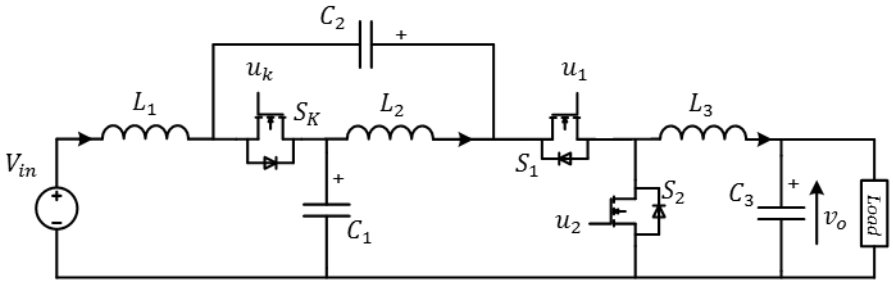


Figure 3 Topologie proposée de convertisseur DC/DC Quasi Z-Source step up/down.

La topologie proposée est composée d'un convertisseur Quasi Z-Source et un convertisseur Buck (QZSBC), comme montré en Figure 3. Le QZSBC proposé est une topologie intéressante lorsque la conversion de tension est requise pour un mode principalement abaisseur. En effet, l'application du cycle de fonctionnement d'un actionneur starter nécessite une faible vitesse du moteur pour la plupart du temps, donc la partie de conversion DC/DC doit fournir principalement une faible tension de sortie. Pendant une brève partie de toute la période du cycle, le convertisseur fournit une tension de sortie élevée afin de permettre à l'actionneur d'atteindre des vitesses plus élevées. De plus, la version à inductances couplées de la topologie permet de supprimer l'ondulation du courant d'entrée à la fréquence de commutation, ce qui apporte un grand gain de masse sur la conception du filtre d'entrée. Un prototype de convertisseur de 3 kW a été réalisé et les résultats expérimentaux montrent sa faisabilité.

Le convertisseur QZSBC a été comparé à un convertisseur SEPIC classique. Cette topologie a été choisie en raison de la caractéristique commune concernant le courant d'entrée continu et la possibilité de supprimer l'ondulation du courant d'entrée. La comparaison a été menée afin de montrer les contraintes de tension et de courant dans les composants actifs et passifs des convertisseurs pour une gamme donnée de gain de tension. La quantité d'énergie magnétique et électrostatique stockée par les composants passifs montre que la QZSBC stocke moins d'énergie, ce qui signifie que, en raison de la relation entre l'énergie stockée et la taille des composants passifs, la QZSBC nécessite des condensateurs et des inductances plus petits pour la plage de fonctionnement considérée. En outre, l'analyse des

courants efficaces et des tensions inverses sur les dispositifs à commutation dure suggère que les pertes de puissance dans le convertisseur proposé sont plus faibles pour la plage de fonctionnement en mode abaisseur et comparables pour le mode élévateur. Par conséquent, l'efficacité du QZSBC mesurée sur un cycle de mission entier sera supérieure à celle du SEPIC, ce qui signifie que le convertisseur a globalement de meilleures performances dans l'application mentionnée.

Les principales exigences pour l'application d'entraînement moteur décrite sont clairement la compacité et l'efficacité. Cependant, le problème de conception d'un convertisseur DC/DC n'est pas une tâche triviale, surtout lorsqu'il s'agit d'optimiser des performances multiples. Plusieurs variables relatives à chaque composant sont impliquées, qui appartiennent à différents domaines d'ingénierie (électrique, magnétique, thermique...). De plus, la plupart des variables sont liées les unes aux autres. Pour atteindre différents objectifs (efficacité et compacité), le concepteur doit avoir une connaissance approfondie de l'influence de chaque variable de conception, afin de faire les compromis appropriés et de respecter les contraintes de faisabilité et d'application. Il convient de noter que les paramètres de conception sont par ailleurs restreints à la disponibilité des composants sur le marché. Dans le chapitre 3, le problème de conception de la partie de puissance d'un convertisseur Boost (Figure 3) et de son filtre d'entrée est décrit pour chaque élément.

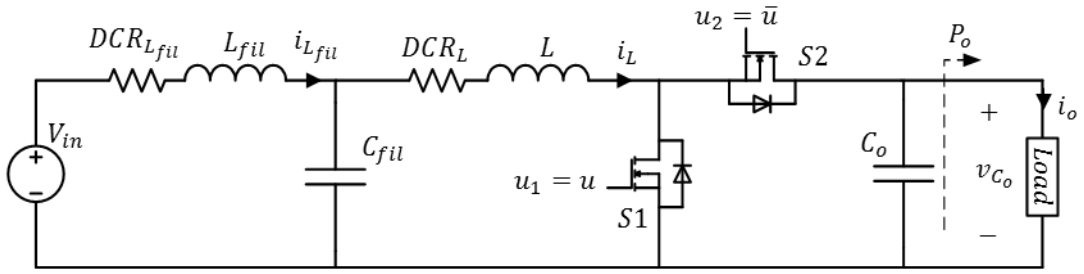


Figure 4 Convertisseur Boost DC/DC et filtre d'entrée différentiel.

Les modèles analytiques utilisés, les variables et les paramètres relatifs sont présentés afin de comprendre les compromis impliqués dans la conception de l'étage de puissance du convertisseur. Dans ce chapitre, les principaux éléments d'un convertisseur ont été abordés et leur rôle et leur impact sur les performances du convertisseur ont été analysés. Les paramètres de conception des composants et les modèles de performances présentés seront précieux pour le chapitre 5 afin de réaliser une optimisation globale du convertisseur.

Un aspect souvent pris en compte est le comportement dynamique du convertisseur, tel que la réponse à une variation du point de fonctionnement ou à une perturbation, malheureusement il est fréquemment envisagé après la conception de la partie puissance du convertisseur. Dans l'application considérée du groupe motopropulseur, si le moteur doit fournir un échelon de couple, le courant requis par le convertisseur augmente fortement en raison du contrôle rapide des courants de phase du moteur. Un tel appel de puissance de charge pourrait provoquer une chute de la tension de sortie du convertisseur DC/DC, ce qui pourrait affecter la contrôlabilité des courants de phase. La réponse dynamique de la tension de sortie du convertisseur aux variations de la charge de puissance ne dépend pas exclusivement de la stratégie de contrôle et de ses paramètres, mais aussi des composants et des paramètres de l'étage de puissance, tels que les composants passifs et la fréquence de commutation. Comme présenté dans le chapitre 4 à travers les principes fondamentaux de la théorie des systèmes linéaires, les éléments passifs du convertisseur ont une forte influence sur le comportement dynamique du convertisseur, ~~puis~~ et sur la conception du contrôleur et la stabilité du système. De plus, en raison des limitations pratiques des régulateurs (bande passante finie, saturation des signaux de commande), l'excursion des courants/tensions des composants passifs ne peut être réduite en dessous d'un certain niveau. Les composants passifs doivent être spécifiquement conçus pour assurer la pleine conformité avec le cahier des charges et les contraintes sur l'excursion de courant et tension aux bornes d'entrée et de sortie du convertisseur lors des variations du point de fonctionnement prévue dans le cycle de la mission.

L'analyse dynamique a été menée pour le convertisseur Boost DC/DC, et le système a été caractérisé au moyen d'une modélisation des petits signaux. L'analyse de la fréquence des fonctions de transfert du convertisseur a montré des limitations dynamiques dues au zéro dans le demi-plan droit, commun à toutes les topologies dérivées du convertisseur Boost. Ce problème est un facteur limitant pour la stratégie de contrôle du convertisseur. Il a été démontré que le choix d'une stratégie de commande à boucle unique est inadapté à la gamme de valeurs des paramètres du circuit (fréquence de commutation, valeurs de capacité et d'inductance) habituellement considérés pour de telles applications. Une stratégie à deux boucles, comme dans le schéma de contrôle en Figure 5, est plus appropriée, elle permet également de contrôler le courant de l'inducteur et de contenir sa variation.

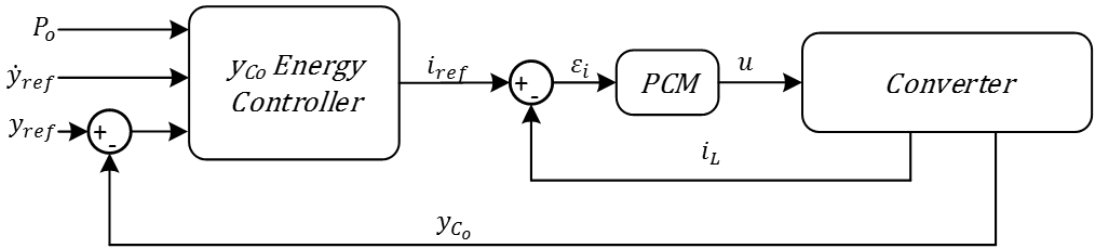


Figure 5 Schéma de contrôle à double boucle, avec régulation d''énergie.

Quant à la boucle de courant interne, un régulateur de courant pic a été retenu en raison de sa robustesse, de sa rapidité et de son utilisation répandue dans ce type d'applications.

La tâche principale étant de contenir la variation de la tension de sortie lors d'une éventuelle variation de la puissance de sortie, une stratégie de contrôle se caractérisant par un meilleur rejet des perturbations de la charge de sortie a été proposée pour la boucle de contrôle externe. Ce régulateur contrôle l'énergie stockée dans la capacité de sortie, donc la tension de sortie indirectement.

Si le contrôleur assure une bonne immunité aux perturbations de la charge, le condensateur de sortie ne doit pas être surdimensionné pour contenir l'excursion de la tension de sortie. À cet égard, une méthode analytique de conception du condensateur de sortie a été proposée afin de maintenir la tension de sortie inférieure/supérieure du système contrôlé pendant les transitoires de puissance de charge dans les limites d'excursion de tension. La valeur minimale de la capacité obtenue dépendra des paramètres du point de fonctionnement, de la fréquence de commutation, de la valeur de l'inductance et des paramètres du contrôleur également.

Dans la dernière section du chapitre 4, la question de la stabilité est abordée. En raison de la haute performance dynamique du régulateur de courant d'entrée du convertisseur, le comportement dynamique de l'ensemble de l'actionneur peut être considéré comme une charge à puissance constante avec impédance négative, ce qui pourrait conduire à des problèmes d'instabilité. L'interaction entre le système en boucle fermée et le filtre d'entrée a été analysée dans le domaine linéaire dans une première approche, en particulier en analysant l'impédance d'entrée du système en boucle fermée et l'impédance de sortie du filtre affecte les pôles du système global. Cette méthode, même si elle est largement utilisée, ne permet pas d'inclure les effets non linéaires dus au comportement de commutation du système réel. Pour cette raison, un outil plus fiable a été développé pour analyser la stabilité du système même pour des fréquences proches à cela de découpage. L'approche consiste en un modèle discret du système en régime permanent pour en déduire sa matrice dynamique (Jacobienne). L'évolution temporelle du système discret est cohérente avec celle du système à temps continu en simulation (Figure 6), ce qui prouve la fiabilité du système obtenu.

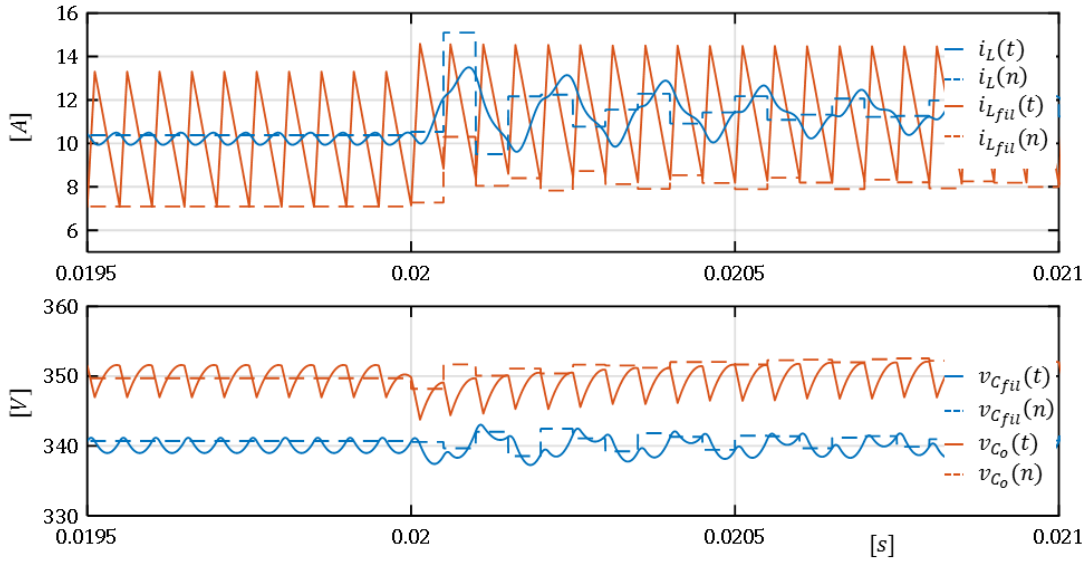


Figure 6 Comparaison entre la simulation à éléments réels et le modèle discret développé.

L'analyse des valeurs propres de la matrice permet de vérifier la stabilité du système composé par le filtre d'entrée LC, le convertisseur DC/DC et une charge de puissance constante. Cet outil est plus susceptible d'être inclus dans une routine d'optimisation, comme indiqué dans le chapitre 5.

Alors que l'optimisation de la compacité et de l'efficacité du seul circuit électrique du convertisseur était une tâche non triviale, elle est encore plus compliquée si l'on tient compte du comportement dynamique, y compris la stratégie de contrôle et les paramètres respectifs. Afin d'aborder les nombreuses variables et paramètres impliqués dans le problème de l'optimisation (de la partie puissance et du contrôleur), un outil d'optimisation multi-objectifs a été développé dans le chapitre 5. Grâce à la procédure proposée, les solutions de dimensionnement les plus avantageux en termes d'efficacité et de compacité sont identifiées.

Outre le comportement en régime permanent, l'algorithme développé tient compte de la dynamique du convertisseur pendant la variation de la puissance de la charge. Cela signifie que l'évaluation des solutions implique la sélection simultanée des paramètres de l'étage de puissance et du régulateur, ce qui garantit une conception optimale capable de répondre aux spécifications tant en régime permanent qu'en régime transitoire. En outre, la stabilité du système composé du convertisseur, de la charge et du filtre d'entrée est également assurée.

Dans le chapitre 5, les limites des approches de conception traditionnelles pour les convertisseurs de puissance ont été discutées, en particulier lorsque l'optimisation de performances multiples est nécessaire. Les outils les plus utilisés pour la résolution d'un problème d'optimisation multi-objectifs dans le domaine de la conversion de puissance consistent en des algorithmes stochastiques, basés sur des procès évolutifs. En particulier, les principes fondamentaux d'un problème multi-objectifs ont été introduits et l'approche de résolution basée sur un algorithme génétique élitiste a été discutée. Plus précisément, un algorithme génétique non dominé a été utilisé (non-dominated sorting genethic algorithm, NSGA-II), ce qui garantit à la fois la convergence et la diversité des solutions de dimensionnement. Après une brève introduction de la structure et des principales étapes de la NSGA II, le problème de conception du système composé d'un convertisseur DC-DC boost de 3kW et du filtre d'entrée différentiel a été formulé afin de s'adapter à la procédure d'optimisation. Ainsi, l'objectifs et les fonctions de contraintes ont été définis selon les modèles des composants du convertisseur décrits dans le chapitre 3. Les variables de conception considérées ont été choisies de manière opportune en fonction du degré de liberté du problème et afin de tenir compte de la disponibilité commerciale des composants sur le marché. Les spécifications de conception comprennent la limite d'excursion de la tension de sortie à la fois en régime permanent et lors d'événements transitoires de la puissance de charge, et les exigences

de la norme DO-160 à basse fréquence sur l'ondulation du courant d'entrée en régime permanent. Le convertisseur alimente un charge a puissance constante (constant power load, CPL), qui représente le cas le plus défavorable en termes de stabilité. Dans la littérature, les optimisations proposées pour les convertisseurs visent à développer des procédures de conception uniquement pour le mode de fonctionnement en régime permanent ; le comportement dynamique en cas de perturbations ou de variations du point de fonctionnement est souvent négligé dans la phase de dimensionnement. Dans la méthode proposée, puisque le convertisseur est conçu pour résister à d'éventuels transitoires de puissance de charge, la stratégie de contrôle et ses paramètres ont été inclus dans la routine d'optimisation. En outre, en raison de la présence du filtre LC d'entrée, l'algorithme d'optimisation inclut l'étude de la stabilité du système au moyen de cycles limites et écarte les solutions de conception instables. L'algorithme trouve les solutions de conception optimales, qui constituent le meilleur compromis entre le volume et les pertes de puissance, indiqué sur le Front Pareto en Figure 7.

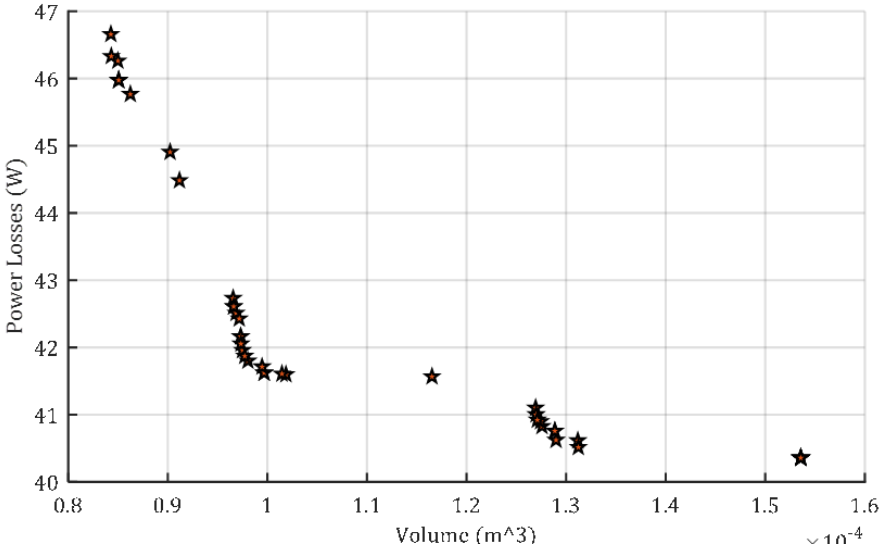


Figure 7 Pareto Front obtenu de l'algorithme d'optimisation exécutée pour un convertisseur boost pour un point de fonctionnement $V_{in} = 270V, V_o = 350V, P_o = 3kW$.

Les solutions obtenues ont été analysées afin de mettre en évidence les valeurs optimales des variables de dimensionnement et le compromis qui en résulte. Les fronts de Pareto obtenus par l'algorithme génétique montrent qu'il est possible d'augmenter les performances du convertisseur par un choix approprié des paramètres du circuit de pilotage des transistors. En outre, les résultats évalués montrent comment le profil transitoire de la puissance demandée affecte le volume des solutions de conception optimales. Afin de démontrer la stabilité du système, la faisabilité des solutions de dimensionnement et le respect des contraintes et de la valeur des pertes attendues, un convertisseur de 3kW à hauts rendement et compacité correspondant à l'une des solutions a été conçu (Figure 8).

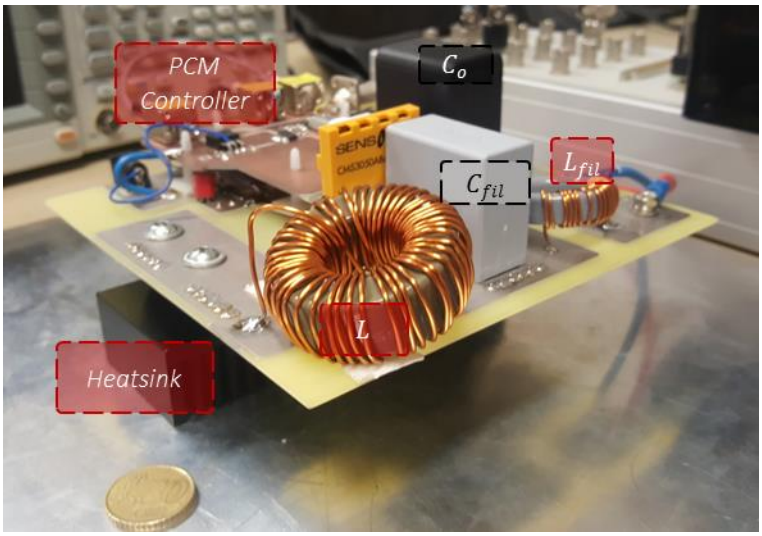


Figure 8 Prototype du convertisseur boost réalisé.

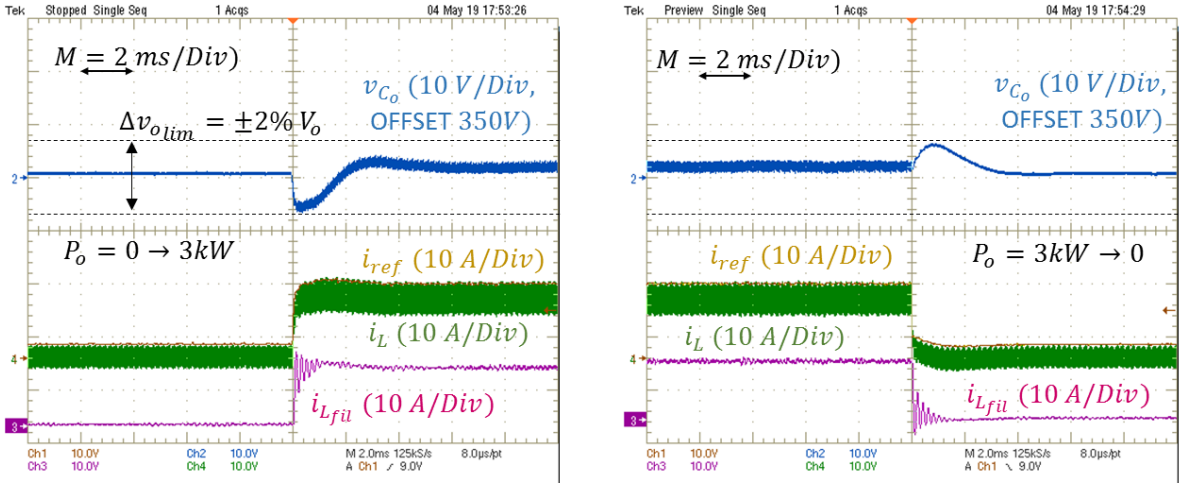


Figure 9 Formes d'onde de la tension de sortie v_{C_o},courant de référence i_{ref}, courants des inducteurs i_L et $i_{L_{fil}}$ pendant les transitoires de charge de montée et de descente.

Les tests expérimentaux confirment la conformité à toutes les exigences et, par conséquent, valident l'efficacité de la procédure d'optimisation proposée. Les performances du prototype du convertisseur boost montrent un bon accord avec les résultats attendus, tant en régime permanent qu'en régime transitoire. Le système contrôlé est stable et les formes d'onde montrent une conformité aux spécifications de tension et de courant lors d'une variation de la puissance de la charge, visible en Figure 9. De plus, les pertes de puissance mesurées confirment le modèle de pertes de puissance adopté.

Contents

General Introduction

Due to the progressive shortage of fossil fuels and the environmental emergency, international agreements have been established to contain the global average temperature growth in the long term. The directives introduced aim to converge financial flows towards a climate-resilient development and to drive the efforts of the industrial community towards a low level of greenhouse gas emissions, especially in the transportation sector, which showed the highest increase rate of energy consumption (then of greenhouse gas emissions) in the last three decades.

The aeronautics and automotive industry moved toward more efficient and autonomous solutions, which led to a considerable electrification of the energy conversion systems on-board. The market of the electric vehicles or hybrid electric vehicles is in consistent growth. The energy exchange between the storage units, the powertrain actuation system, the internal combustion engine/generator and the numerous utility loads is carried through a DC network, and each source/load requires a specific converter to be interfaced on it. At the same time, in the electrical network of the modern aircraft network (More Electrical Aircraft), several mechanical units have been replaced by electrical counterparts, for the benefit of efficiency and weight of the overall system.

To supply the several power loads on-board, the power electronics units consist of switched-mode power converters whose operation take place through the switching of semiconductor transistors. The evolution of the power converters improves simultaneously with the technological progress of semiconductor devices. As explained in the first chapter, silicon-based devices dominated the market in the last three decades. For application within the power range of the order of hundreds of kW, the Insulated-gate bipolar transistor (IGBT) has been the most commonly used device because of its high current and voltage ratings (compared to the MOSFET unipolar devices). Nonetheless, due to the bipolar nature of the IGBT structure, the operating switching frequency of the power converter, when this device is employed, is limited by the commutation times of the device. On the other hand, research on wide band-gap (WBG) semiconductor materials has led to the introduction of new high-performance devices mature enough to make their way into the market. The features of the WBG materials like Silicon-Carbide or Gallium-Nitride allow building unipolar devices, like metal–oxide–semiconductor field-effect transistor (MOSFET), with the same current and voltage ratings of the off-the-shelf IGBTs, higher operating temperature, lower conduction losses and faster commutation times. The possibility to significantly increase the switching frequency while keeping power losses low leads to an overall improvement of the conversion system in terms of efficiency and size of the passive elements and the cooling system. The spread of such devices offers clear opportunities to considerably improve the conversion power electronics systems.

The electrical micro-grids in embedded applications, such as HEV/EV or modern aircrafts, are composed by several electric loads and sources connected to a common voltage bus. The electrical power is usually provided by generator units powered by the combustion engine and storage units (batteries or super capacitors). The maximal power flow in this grid is comparable to the power of the most demanding loads. In case of large variations of the power demanded by the most powerful loads, the voltage provided by the storage units may exhibit a significant variation. This variation affects the design of the several loads connected to the network and usually leads to an increase in volume and mass of the entire embedded system.

The first example concerns the electric energy distribution network aboard a modern aircraft. It is composed of an AC voltage bus and a DC voltage bus supplied by the AC network through rectifier units. In the specific case of the More Electrical Aircraft, the most remarkable evolution is the suppression of the gearbox unit (IDG for Internal Drive Generator), which ensured a fixed mechanical speed for each network connected generator, regardless of the highly variable speed of the engine. In absence of the IDG, the aircraft electrical generation systems are more reliable, but the 3-phase AC

networks have a variable frequency as well as a variable voltage amplitude. The variable amplitude and frequency of the AC voltage causes a consistent variation in the DC bus voltage obtained by rectifier units. Then, the electrical and mechanical loads are supplied by DC/DC or DC/AC (depending on the load) converters connected to variable DC bus voltage.

Similar issues can affect the electrical network of electrical or hybrid electrical (EV/HEV) vehicles, where the DC bus may exhibit large variations because of the non-ideal features of the storage units.

In this context, the efficiency, the size and the level of integration of the power electronics conversion are primary goals to attain. For an embedded powertrain application, the power electronics stage is often composed of just an inverter connected to the DC bus through an input filter, which supplies a poly-phase electrical machine. The DC bus voltage variations affects the motor turn number and its rated current, then the inverter power losses and the inverter cooling unit as well. Indeed, if the drive chain is only composed of the inverter and input filter, the motor stator windings should be designed to operate to ensure the controllability of the motor torque for the whole range of variation of the DC bus voltage value, resulting in increased power losses in the inverter and a consequent oversizing of its active components and cooling unit. As explained in Chapter 2, an interesting alternative to avoid these constraints is to insert a DC/DC converter between the filter and the inverter. This solution helps the inverter's immunization against the voltage disturbances on the DC bus, especially in the case of an electric network in a modern aircraft or in electrical or hybrid vehicles. The additional DC/DC converter offers the possibility to optimize the actuation chain efficiency in the whole operating speed range. Depending on the speed requirements, the best solution could be a step-up, a step-down or a step-up/down converter (for a wide speed range). In Chapter 2, the most common DC/DC converter topologies for such application are presented. For the specific case of wide speed range applications, an original step-up/down topology is presented and analysed.

The major requirements for the described motor drive application are clearly compactness and efficiency of its constituents. However, the design problem of a DC/DC converter is not a trivial task, especially when it comes to optimizing multiple performances. Several variables relative to each component are involved, which belong to different engineering domains (electrical, magnetic, thermal…). Moreover, most variables are inextricably linked to each other. To attain different goals (efficiency and compactness), the designer should have a comprehensive knowledge of the influence of each design variable, in order to make the appropriate trade-offs and comply with the feasibility and application constraints. It should be remarked that the design parameters are limited to the availability of the components on the market. In Chapter 3, the design problem of a DC/DC power stage (boost converter and input filter) is described for each element. The analytical models employed and the relative variables and parameters are presented in order to understand the compromises involved in the design of the power stage of the converter.

One aspect often considered only after the design of the converter power stage is the dynamic behaviour of the converter, such as the response to a variation in the operating point or a disturbance, such as load variation or DC-bus voltage variation.

In the considered powertrain applications, if the motor torque, then the motor phase current references, need to increase quickly, the motor phase currents will rapidly increase as well, due to wide bandwidth of the current control loops. Under such condition the inverter power step could cause a drop of the DC/DC converter output voltage, which may affect the controllability of the phase currents. The dynamical response of the DC/DC converter output voltage to power load variations does not depend exclusively on the control strategy and its parameters, but also on the power stage components and parameters, such as the passive components and the switching frequency. As discussed in Chapter 4 through fundamentals of linear system theory, the passive elements of the converter have a strong influence on the dynamical behaviour of the converter, then on the design of the controller and the system stability. Furthermore, due to the practical limitations of the regulators (finite bandwidth, command signals saturation), the excursion of the passive components' currents/voltages cannot be reduced below a certain level. Passive components should be specifically designed to ensure full

compliance with the input and output terminal excursion requirements of the application during any variation of the operating point scheduled in the mission cycle.

For the case under study, the control strategy has been chosen specifically for the rejection of the power load variations. Once the control strategy and the controller parameters have been defined, the closed loop system stability can be analysed, especially when an input filter is required for the input current harmonics to meet the standards imposed by the application. In fact, the interaction between two cascaded stable subsystems, as in the case of the input filter and the converter, can lead to instability. The stability issues of the system composed by the converter and the input filter are discussed in Chapter 4 as well.

While optimising the compactness and efficiency of the converter's power circuit alone was a non-trivial task, it is even more complicated if the dynamic behaviour is taken into account, including the control strategy and the respective parameters. In order to address the numerous variables and parameters involved in the optimization problem (of both power stage and controller), a multi-objective optimization tool has been developed in Chapter 5. Thanks to the proposed procedure, the most convenient design solutions in terms of efficiency and compactness are identified.

Besides the steady state behaviour, the developed algorithm takes into account the dynamic of the converter during the variation of the load power. This means that the evaluation of the solutions involves the selection of the power stage and regulator parameters at the same time, ensuring an optimal design that is able to meet the specifications both in steady state and in transient behaviour. Furthermore, the stability of the system composed by the converter, the load and the input filter is ensured as well. A 350V/3kW test bench has been implemented to validate the reliability of the models employed in the routine and to verify the compliance with the design specifications of the converter prototype in steady state and load transient.

1 Power Electronics Systems for Embedded Applications

1.1 Introduction

This chapter is meant to introduce the context of this work. The main objective of the thesis is to propose a design approach for a DC/DC converter. The converter is part of the conversion chain for the power supply of an on-board actuator. It has been conceived more specifically for embedded applications in the transportation sector, namely hybrid/electric vehicles and modern aircrafts.

The design targets depend on the requirements of these applications, hence it is fundamental to properly introduce the context in which the design procedure will be developed.

In embedded systems, especially in the domain of the transportation sector, the current trend, due to both the shortage of fossil fuels and the new international agreements for the resolution of pressing environmental issues such as pollution and climate change, is to reduce the green-house gas emissions.

Moreover, in on-board electrical systems, as in the most aircraft electrical networks, several hydraulic, pneumatic or mechanical parts have been replaced by electrical counterparts, which leads to a remarkable gain in terms of size, weight and wasted power.

Since the storage systems and the utility power loads on-board operate at DC voltages, the design of the DC conversion chain within the electrical micro-grid embedded architecture gained a particular attention. In this context, the main elements of the electrical grid in electrical and hybrid electrical vehicles and modern aircraft are described in the following.

Currently, the electrical network on-board in most vehicles includes at least one DC bus, in which the DC/DC conversion is largely employed, as it will be showed in the following. The current tendency is to push the operating voltages toward higher values, which leads to a significant gain in terms of efficiency and size of the conversion system.

In order to follow the increasing trend of power electrical need, the on-board converter should be designed as small and as efficient as possible, so to lighten the conversion chain and reduce the fuel consumption. The achievement of such objectives could be pretty challenging, especially when the design problem is constrained by the ripple requirements set by the aeronautics or automotive standards. The energy storage or supply devices, indeed, may vary their output voltage in response to variation of the load or their state of charge. Such variations should comply with the requirements of the standards in order not to compromise the normal functioning of the other devices connected, or even the stability.

In the last decade, the availability on the market of wide band-gap semiconductor devices strongly contributed to the efficiency and the compactness of switched converters, particularly in view of the increase of the voltage values involved. The superior features of these devices provided the opportunity to develop power converters with performances never reached before. Their benefits over the widespread and mature classical devices are discussed in this chapter, and the performances are validated on an experimental test-bench.

1.2 Embedded application in the transportation sector

In recent years, fossil fuel shortage and environmental pollution moved the research community toward more efficient and alternative solutions in the energy conversion field. In order to cope with climate change due to harmful and increasing gas emissions due to the widespread use of fossil fuels, the power and traction architectures of the main transport systems have been revised and improved. The increasing usage of conventional combustion engines is causing harm to the environment and health itself, as these engines burn petrol, diesel or natural gas and produce carbon dioxide (CO_2), Sulphur dioxide (SO_2) and oxides of nitrogen (NO_x) as harmful exhaust components.

As stated in the 2019 annual report by European Environment Agency's European Topic Centre on Climate Change Mitigation and Energy, in the EU, the transportation sector alone is accountable for approximately a quarter of greenhouse gas emissions as illustrated in Fig. 1.1 [1]–[3].

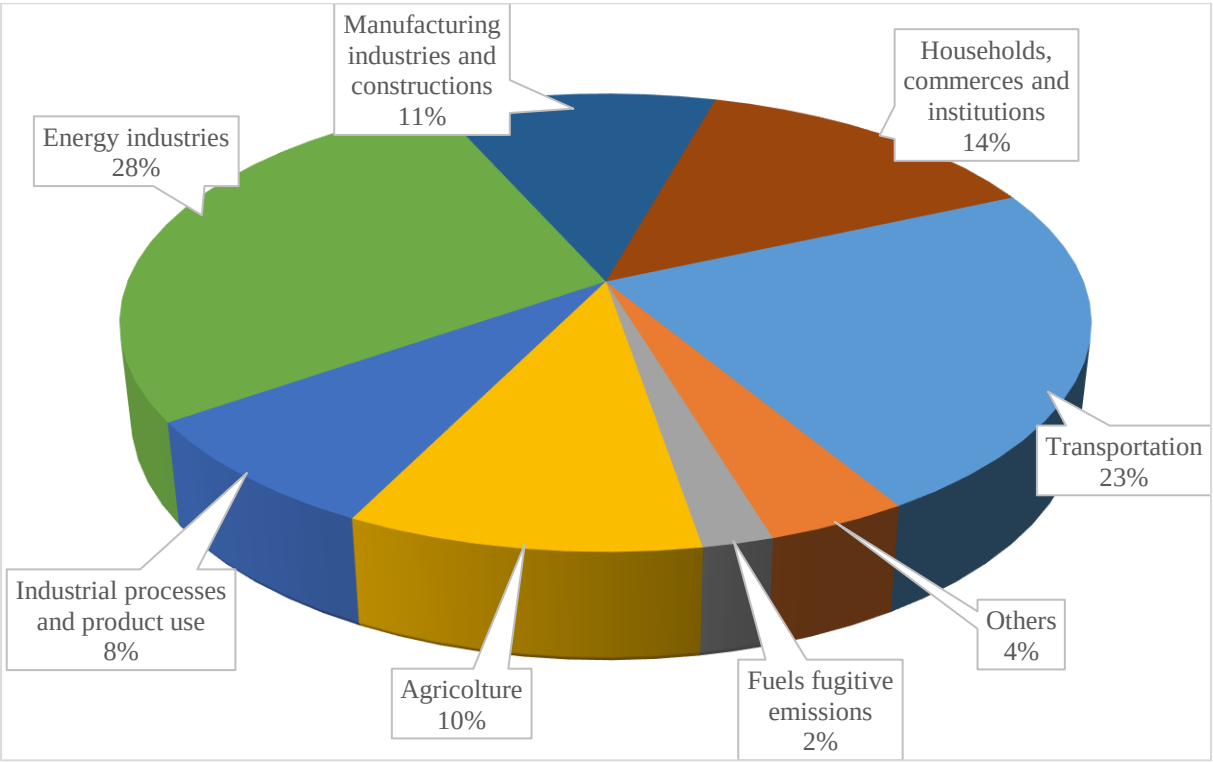


Fig. 1.1 Greenhouse gas Emission reported for the 2019 [4].

Furthermore, it has been registered that greenhouse gas emissions decreased in the majority of sectors between 1990 and 2017, with the notable exception of transport sector, including international transport, refrigeration and air conditioning. The energy consumption, hence the emissions, in the transportation sector exhibited an increase up to 36% in the same period [1], [3], [5], [6].

In order to satisfy the climatic target and the regulations imposed by the international agreements, such as the "Paris Agreement" in 2015 and the "Doha Amendment to the Kyoto protocol (2012)", more electrical alternatives are replacing the conventional drive traction and on-board power supply systems. This imposes new challenges for energy generation, conversion and delivery tasks in the on-board power grid of the means of transport, which lead to the rapid penetration of power electronics systems.

The research effort recently focuses basically into finding miniaturized, lightweight, highly power dense solutions. This allows a reduction in the installation cost, and an improvement of the autonomy of the vehicle. In the following sections, it will be shown the fundamental role of the power electronics conversion in two largely discussed embedded applications, such as the aerospace and the hybrid-

electric vehicles, with a clear emphasis on the role of the DC-DC conversion, which is the subject of this thesis study.

1.2.1 More Electric Aircraft (MEA)

Over the last few decades, there has been tremendous progress and efforts to move toward more electric aircraft (MEA). Considerable effort has been spent in the intensive development of the electrical system on-board of large civil aircraft by Boeing and Airbus, or military aircraft (F-22 or F-35). The MEA has ambitious objectives in the coming years such as reducing fuel consumption and the emissions of noise and gas (CO_2, O_x). It has been estimated, indeed, that 1 kg saved on each flight could save about 1,700 t of fuel and 5,400 t of CO_2 emissions per year for the recent air traffic. In addition, a decrease in mass would also result in a significant gain in cost: every additional kilogram of system costs approximately 1,000 $ [7].

In a MEA, the electrical power supplies the non-propulsive aircraft systems/loads, which are typically driven by a combination of different secondary power types such as mechanical power, pneumatic and hydraulic and so on [8]–[11]. Currently, for example, the environmental conditioning is supplied through a bleed air system [11], [12], which provides pneumatic power directly drawn from high-pressure hot air extracted from aircraft engines. The removal of the pneumatic system eliminates the need for a bleed air system embedded on the gas turbine, which leads to a significant improvement in the efficiency of the turbine. Other types of loads (braking, pumps) that were earlier powered by hydraulic networks were replaced by electrical loads [13]. As for hydraulic energy, it comes from a hydraulic pump driven by the internal combustion engine. This energy is mainly used to operate the flight controls, the undercarriage and braking systems.

The removal of the mechanical and hydraulic systems allows a remarkable reduction of the overall system size. Furthermore, the employ of electrical system remarkably improves the prognostic and diagnostic functions of the system [7], which allows reducing the maintenance time and cost of the aircraft. The first aircraft generations were equipped with fixed frequency (400 Hz) integrated drive generators (IDG), as shown in Fig. 1.2(a). One of the important steps toward the electrification of the aircrafts was the substitution of the IDG by a variable frequency generator. The use of such generator allowed removing the heavy and expensive gearbox system employed to provide the constant frequency.

Two alternative solutions have been proposed. The first option is depicted in Fig. 1.2(b) and consists in a Variable Speed Constant Frequency (VSCF) DC link system [15]. The electrical power supplied by the gas turbine is transformed by a back-to-back frequency converter and brought to a constant frequency of 400 Hz. The AC/AC converter can be realized using several topologies, such as matrix converters, cycle-converters, or back-to-back inverters [16], [17]. The advantage of this solution consists in providing a voltage waveform similar to the classical configuration (115V, fixed 400Hz frequency), which allows to easily adapt the existing loads available on the market. Nevertheless, the presence of the frequency converter implies additional losses and weight, not to mention decreasing the reliability of the system.

Another configuration, as shown in Fig. 1.2(c), represents the preferred solution for recent military and commercial aircraft applications (Boeing 787, Airbus A380), since it is generally characterized by simplicity and reliability. It consists in using directly the AC electrical power provided in a range of frequencies [330Hz;800Hz] and a nominal voltage of 115V or 230V AC [17]. Since most of the electrical aircraft loads requires a controlled constant frequency power supply, the variable-frequency supply cannot be used directly for most applications. That means every load needs its own power converter: this system could be considered non optimal in terms of mass and cost, but it brings several advantages concerning the safety and the failure detections of the single loads [18], [19].

An example of electric grid on-board is shown in Fig. 1.3.

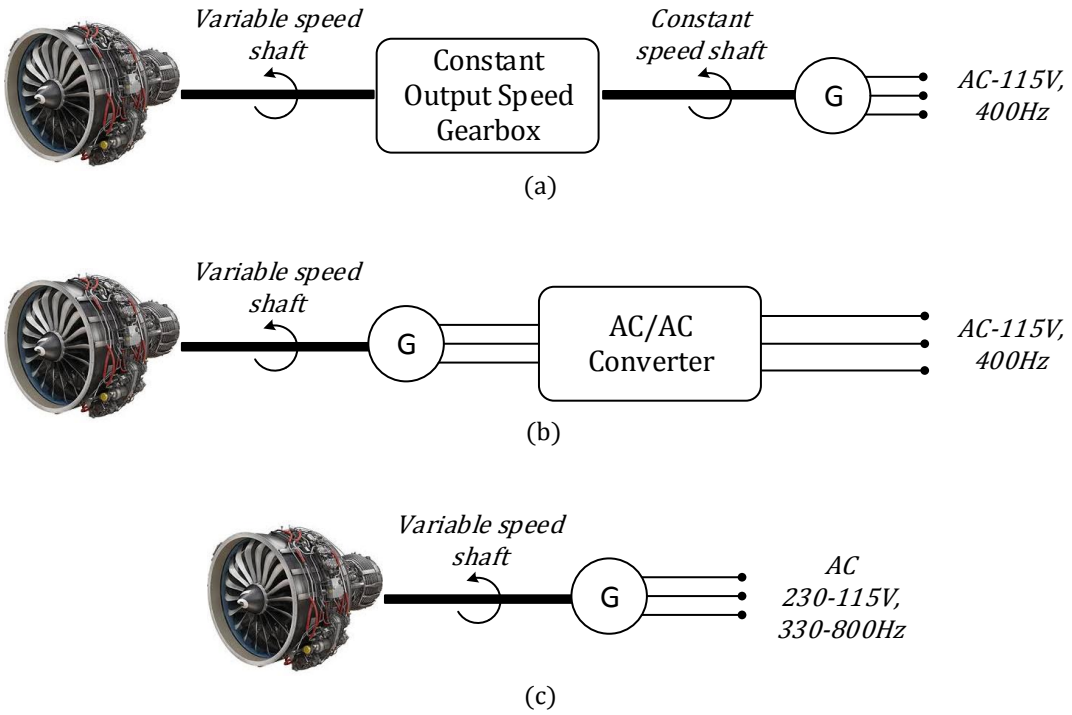


Fig. 1.2 Evolution of the AC electric generation and distribution network [14].

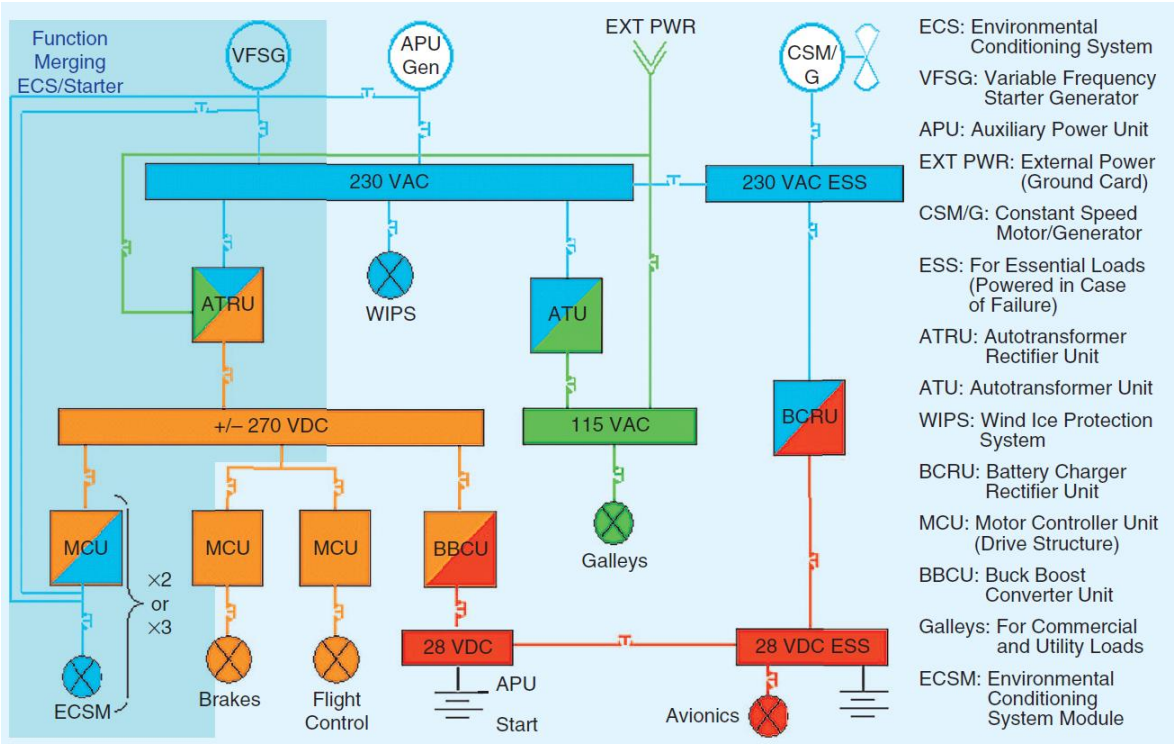


Fig. 1.3 Example of on-board electric grid supplied by a variable speed variable frequency generator [7].

The VSG (Variable Speed Generator) supplies the AC bus with variable frequency and voltage. A conventional aircraft grid is based on a main bus voltage of 115 V AC, but, recently, some newer developments use 230 V AC [7], [17].

Most of the power loads on-board are supplied by a DC voltage, generated from the AC bus through a rectifier unit. The trend is to use a DC link of 270 V (±135 V) or 540 V (±270 V), respectively generated from a 115 V AC or 230 V AC, 330–800 Hz through an auto-transformer rectifier unit (ATRU). For a

DC network with a nominal voltage of 270VDC, it can vary from 230V to 335V because of the variable amplitude of the AC voltage generated by the VSG. A lower voltage bus of 28 V DC is employed to supply the minor loads.

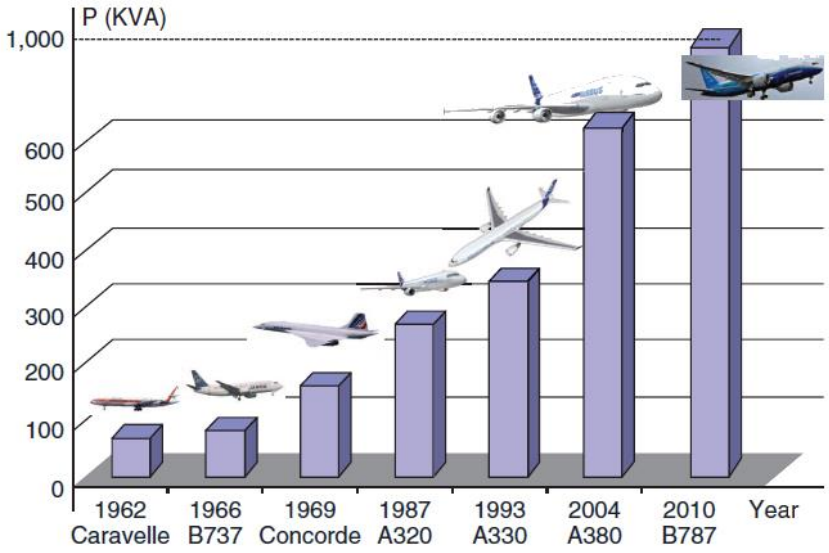


Fig. 1.4 Electrical power demand trend in commercial aircrafts [7].

Fig. 1.4 shows the increasing evolution trend of the electrical power need of a common aircraft over the last fifteen years. With respect to the increase of the loads' power, the trend moved toward high voltage DC network (HVDC). HVDC-grids provide indeed several benefits. The main advantages are manifold.

The current levels are lower (10 times compared to the 28 V DC bus) than the conventional low voltage levels. Hence, the cross-section of the wires can be considerably reduced, as well as the weight.

With the increasing number of power electronic loads, a MEA with a classical AC network would include a high number of AC/DC rectifier stages. A more suitable interface between the grid and the DC loads allow to reduce the weight and the efficiency of the DC/DC conversion systems.

The HVDC network, furthermore, would ease the voltage coupling between the loads and the generator, with possible regenerative load acceptance [20].

A simplified example of the DC power distribution architecture of the DC link system in a MEA is shown in Fig. 1.5. A battery unit is employed primarily to support the starting process of the engine and to power the auxiliary units, or as emergency backup power for equipment and instruments.

The grid showed in Fig. 1.5 consists of a battery storage system, 270 V DC power distribution bus, AC and DC loads and the respective converters. The power generation block consists of the engine Starter/Generator set: it provides the electrical power to the distribution bus, thus powering the electrical loads, during the generation phase. It is connected to the bus through a bidirectional DC/AC inverter, usually decomposed in a DC/DC converter and a Voltage Source Inverter (VSI) inverter. Another bidirectional DC/DC converter interfaces the battery unit with the DC bus. Unidirectional DC-DC converters are commonly used in the grid to supply other utility loads or to 28 V DC and a DC-AC converter is used for conversion to 115 V AC. All the conversion stages shall be designed carefully in order to meet the volume, weight and efficiency requirements for aeronautics applications. Furthermore, they must satisfy the aviation standard, such as DO-160 or MIL-704, which set the harmonic emission standards [11], [21]–[23].

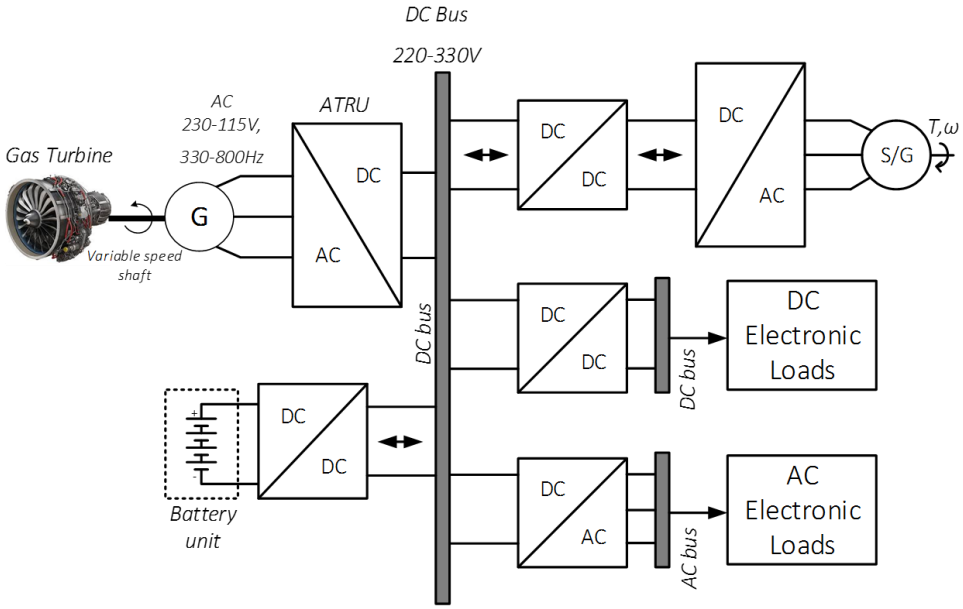


Fig. 1.5 Example of DC micro-grid on-board in a MEA.

1.2.2 EV/HEV

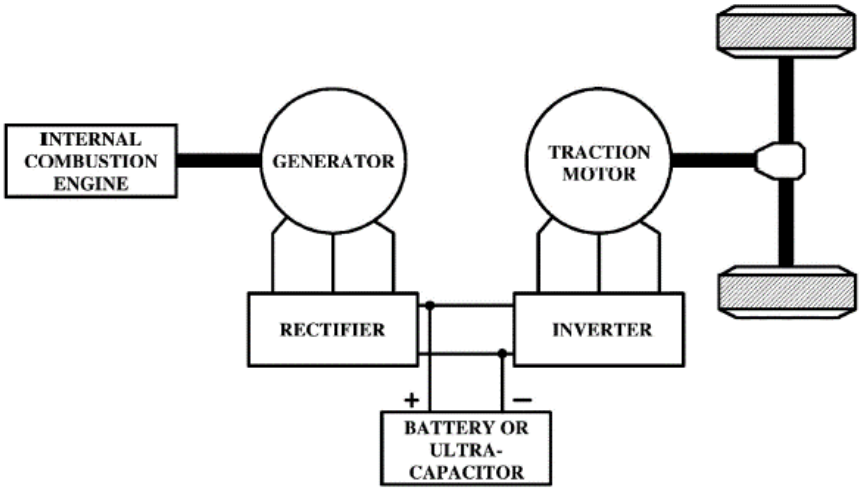
Similarly to the aeronautics field, the automotive industry, pushed by the demands of higher fuel economy and more electric power, is moving toward an evolution of the electrical power systems. Several functions that were traditionally led by mechanical, pneumatic, and hydraulic systems, are now increasingly being replaced by the electrical systems, in order to increase the performance and efficiency [4], [24]. Furthermore, the electrical demand on-board strongly increased because of the introduction of a wide range of new functionality in vehicles. Indeed, the rate of increase of automotive loads is about 4% per year [25].

Due to cost reasons, the market and the industry have recently focused on the production of hybrid electric vehicles (HEV), rather than pure electric vehicles (EV). Between the innovative solutions, it is worth mentioning the fuel cell propulsion system, which represents an interesting alternative compared to the EV, especially for the emission benefits. Nevertheless, the widespread of fuel cell powered systems is impeded by the high production costs and the limited spread of supporting infrastructures and refuelling stations.

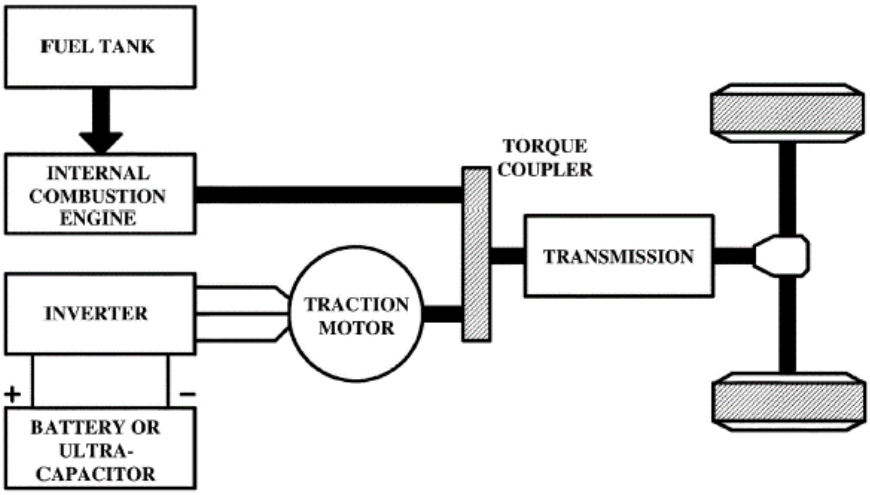
Hybrid vehicles have two or more energy sources. In a HEV the traction is partially sustained by the combustion engine and partially by a battery unit or a super capacitor unit, depending on the configuration [3], [25].

In Fig. 1.6, three among the most used architectures of a HEV powertrain architecture are depicted.

The series configuration Fig. 1.6(a) is the closest one to a pure electric vehicle architecture, where the thermal engine is employed to charge the propulsion batteries/super-capacitor bank on-board the vehicle. The power flow is converted twice by a generator upstream the battery bank and an inverter connected to the electric motor. Contrary to the series set up, the engine/generator in the parallel Fig. 1.6(b) and series/parallel Fig. 1.6(c) configurations is mechanically connected to the transmission block. The advantage of the series HEV configuration is that the fuel engine runs mostly at its optimal combination of speed and torque, having a low fuel consumption and high efficiency. On the other hand, the double conversion stage between the fuel engine and the transmission can cause an important loss of energy. Hence the development of the others configuration, which improve the overall drive train efficiency.



(a)



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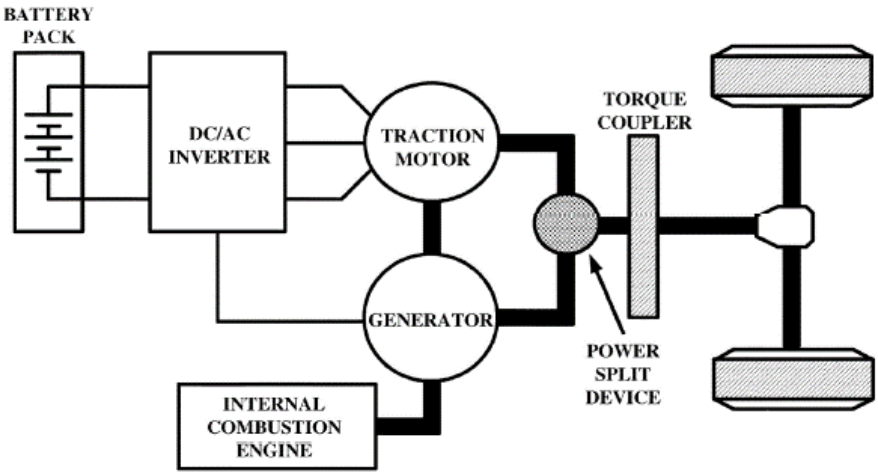


(c)

Fig. 1.6 HEV series (a), parallel (b) and series/parallel (c) architectures [26].

Generally, a series hybrid is preferred when the mission cycle includes frequent start/stops, typically for city employ. A parallel hybrid vehicle offers lower fuel consumption in the highway driving cycle, in which the vehicle is mostly running at constant speed.

In Fig. 1.7 an example of a typical micro-grid architecture on-board is shown [24]. The continuous increase in power requirements motivated the development of both higher-power and higher-voltage electrical systems. The DC bus voltage levels moved from the conventional values of 6V, 12 V to 300V and higher values [27].

The architecture scheme is pretty similar to the one presented for the MEA case. A common use is to employ at least two DC busses, a high voltage (150/300V) main bus for high power loads, and a lower voltage bus for minor DC loads (14/42V) [28].

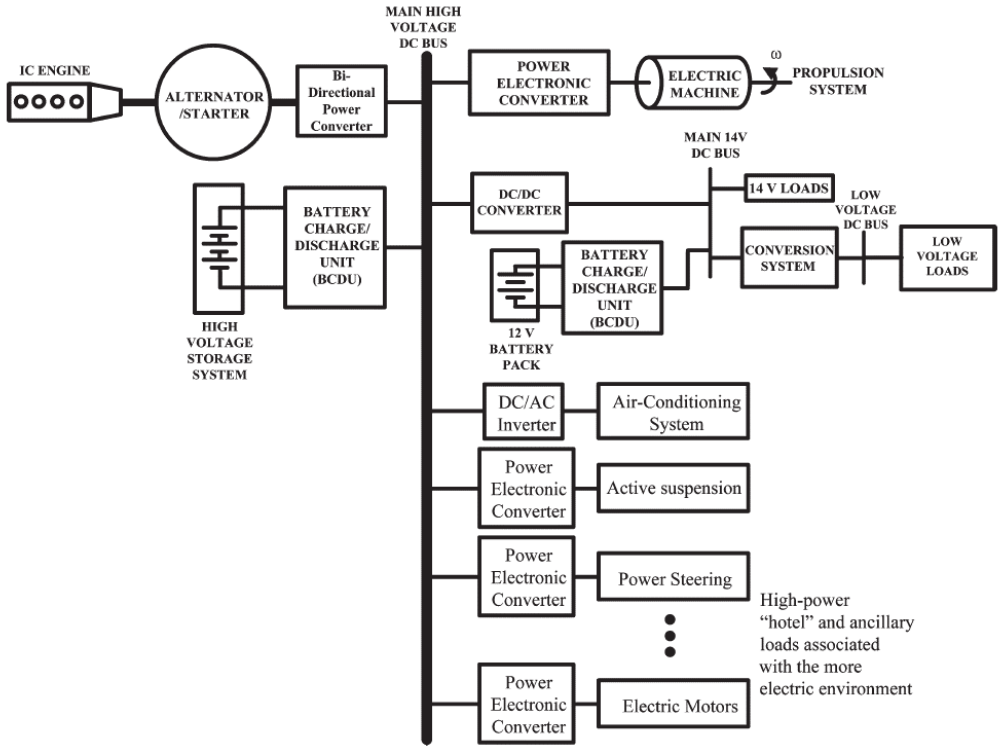


Fig. 1.7 HEV electrical grid example [26].

Unidirectional DC-DC converters supply various low power loads such as sensors, controls, entertainment, utility, and safety equipment. Bidirectional DC-DC converters are used in places where battery charging, regenerative braking, and backup power are required. As a backup power system, the bidirectional DC-DC converter facilitates the safe operation of the vehicle when the internal combustion engine or the electric drives fail to drive the motor. Due to the aforementioned reasons, high power bidirectional DC-DC converters have recently gained a lot of importance. Research in wide band-gap devices is mature enough to attain the increasing demand of small-sized, reliable, lightweight, controllable and efficient DC-DC converters in automotive industries.

1.3 New opportunities: Wide Band-Gaps Devices

It is clear from the review that, in the ranges of voltage and power involved in micro-grid structures for mobile applications, the DC-DC converters are leaning towards fast switching active components.

Therefore, semiconductor materials that help to achieve a higher switching speed that does not correspond to an excessive increase in thermal losses are preferred. Thus, Wide Band-Gap (WBG) materials are quickly becoming the mainstay of high-power and high-speed.

Based on the consideration developed in the previous sections, DC-DC power converters for aeronautics or EV/HEV applications require powerful, compact, and reliable electronic devices in order to facilitate power system integration. In a Switched Mode Power Supply (SMPS), the nature of the semiconductor devices has a heavy impact on the design and the performances of the whole converter.

In most of the switching applications Metal-Oxide Semiconductor Filed Effect Transistor (MOSFET) and Insulated Gate Bipolar Transistors (IGBTs) are predominant than the other switching devices due to the easy driving ability and their specific features (respectively high-power ratings and fast switching behaviour).

These applications include Uninterruptable Power Supplies (UPS), Solar Inverters and Converters, various motor driver systems, Pulse Width Modulation (PWM) technique-based applications, SMPS etc.

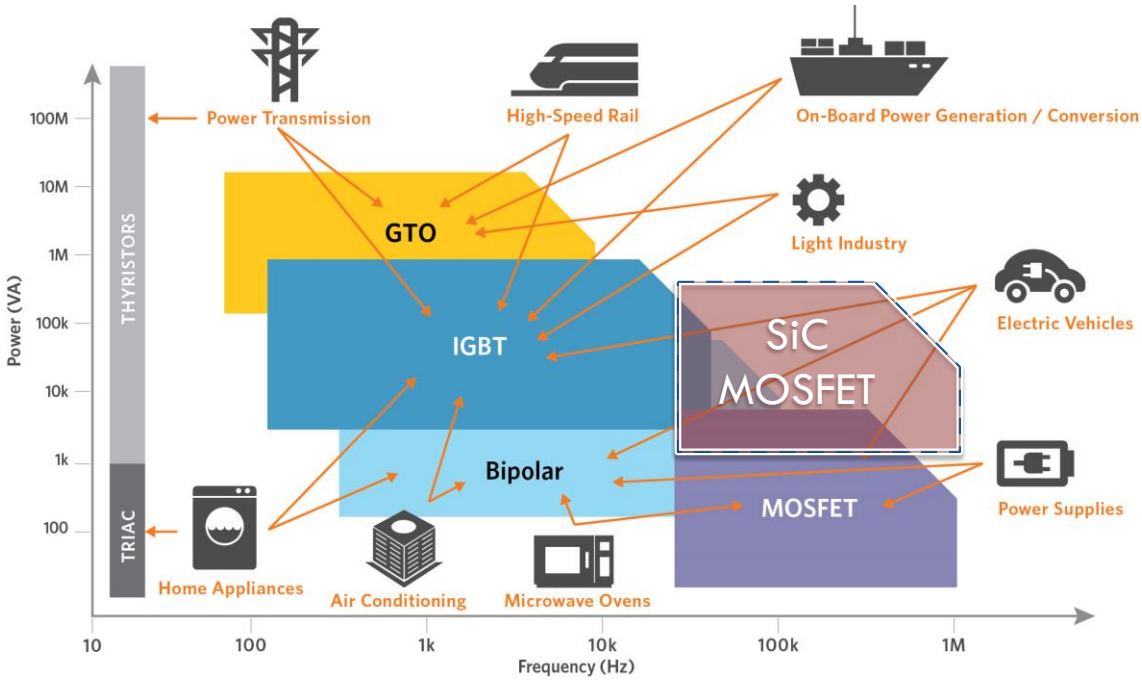


Fig. 1.8 Power/frequency application ranges of the common power devices [29].

For high voltage applications, the silicon Si IGBT has been the dominant power semiconductor device in low and medium frequencies power conversion applications, in power ranges from the kilowatt to the megawatt. In the last 30 years, the research results brought the development of Si IGBT and free-wheeling diode technology to a high level of maturity [30]. The incremental improvements in performances obtained with each new generation of IGBT technology are becoming ever smaller, hence the need of an alternative to the Si technology. Further developments of the performance of Si-based semiconductors is limited by their physical properties and characteristics. The employ of Si-based semiconductors limits indeed the converters efficiency and allows a maximum switching frequency up to 30 kHz, which lead to a limited power density [4], [31]–[33].

The recent advances in WBG technology has created great opportunities for increasing the efficiency and the power density of the conversion chains. Contemporary researches found that silicon carbide (SiC) semiconductors are highly suitable for designing high power DC-DC converters due to its capability for handling vast power ranges up to 100 kW [31]. Most important, SiC features allow to build extremely fast devices able to remarkably increase the operating switching frequency, which brings drastic improvements in the power density of the converter. At the same time, the GaN, is

considered as the future low-cost device [34], [35], even if it still is not mature enough. Its growth in high power applications is currently hold back by several technological constraints, such as packaging and reliability.

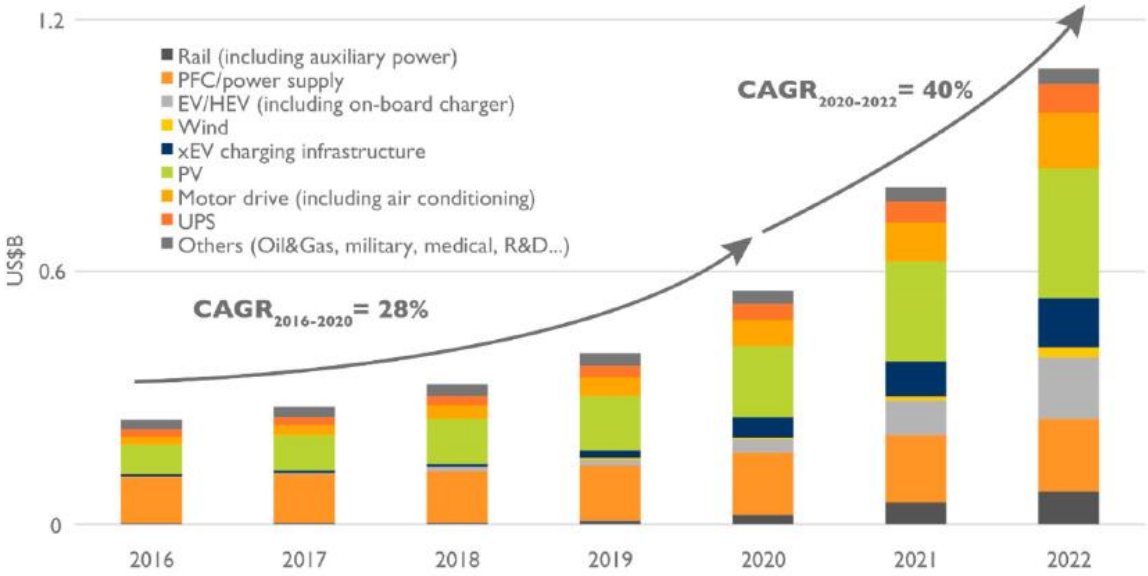


Fig. 1.9 WBG growing market [36].

With the rapid technology innovations and continued advancements in the semiconductor industry, SiC-based power devices have evolved from immature prototypes in laboratories to a viable alternative to Si-based power devices. Many SiC power devices in the kV range are being investigated, such as SiC PiN diodes, Schottky diodes, JFET, BJTs and various MOSFETs. An investigation, carried out by the Yole Developpement Institute [36], concerning the market trend analysis of the WBG devices show a consistent increase of the market profits, as shown in Fig. 1.9, and estimated future revenues are as promising as they have been so far.

1.3.1 SiC and Si technology comparison

Silicon carbide (SiC) potentially offers several advantages over conventional silicon (Si) for use in power electronics devices. Comparatively, individual SiC materials (in theory) can endure temperatures up to 300°C (standard Si is typically limited to 150°C), withstand higher voltage for the same width, tolerate a larger current density, and operate at a higher frequency [37]. Indeed, in switching conditions, SiC MOSFETs show reduced conduction losses and allows low power switching losses. The enhanced efficiency can lead to reduction of cooling requirements and heatsink volumes. Moreover, the better dynamic performance of SiC-based devices allows to obtain high operating frequencies with consequently reduction of weight and size of the power converters' passive components (inductors, capacitors). Furthermore, the increase of the maximal operating temperature of the semiconductor device junction can improve the reliability of the system. Nevertheless, the operating temperature, for MOSFETs and IGBTs, is rather limited by the gate oxide that, contrarily to the JFET, limits the usage to 175°C. Power devices based on SiC have many advantages for high performance (high voltage, high current density, high temperature and high efficient) power electronics converters related to inherent material properties [31], [37].

The main benefit of silicon carbide (SiC) compared to silicon (Si) from a physical point of view is the larger band gap energy (varying from 2.37 eV for 3C-SiC to 3.26 eV for 4H SiC at room temperature). Particularly, the band gap of the most commonly used polytype (4H-SiC) is 3 times larger than silicon, which allows high temperature operations and low leakage current in reverse voltage condition.

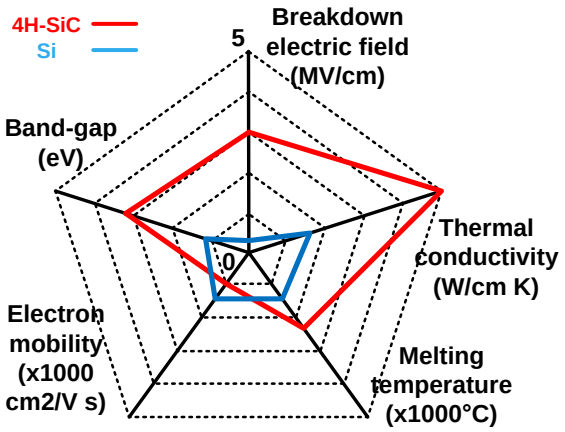
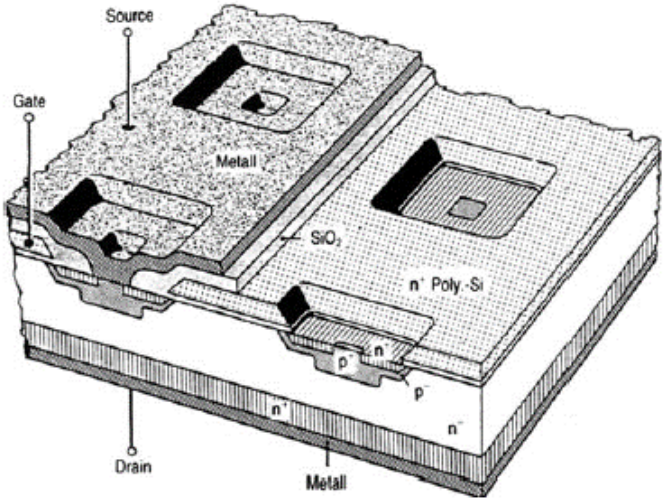
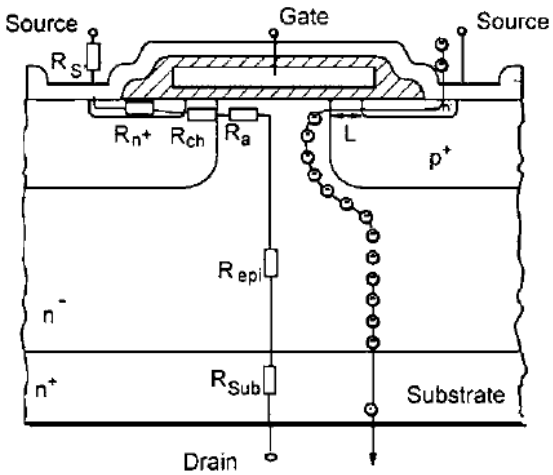


Fig. 1.10 Comparison of the mean features of Si and 4H-SiC materials [37].



(*a*)



(*b*)

Fig. 1.11 3D(a) and cross section (b) of a npn MOSFET structure on a semiconductor wafer [39].

The higher thermal conductivity allows more heat to be dissipated from the SiC based device and a smaller temperature difference with the environment. Moreover, a high critical electric field, an order of magnitude greater than silicon (2.5 MV/cm for SiC-4H against 0.2 MV/cm for silicon). This level of

critical field enables the realization of drift layers with very low specific resistance, as compared to silicon, and therefore of unipolar components (JFET, Schottky diode, MOSFET) with very low series resistance [38].

In Fig. 1.11, the resistive path of the carriers is showed within a MOSFET topology. In the ohmic operating mode of the MOSFET ($V_{DS} \ll V_{GS} - V_T$, with V_T the gate-source threshold voltage), which is the operating zone of a power switching device, the drift region stands for the most part of the resistance (R_{epi} in Fig. 1.11(b)), or also called epitaxial region (since it is produced by epitaxy process). The conduction on-resistance can be approximated as in [31]:

$$R_{on} \cong R_{epi} = \frac{4(V_B + V_{bi})^2}{A\ \mu\ \varepsilon\ E_{max}^3} \tag{1.1}$$

where V_{bi} is the built-in potential, $\varepsilon = \varepsilon_0 \varepsilon_r$ is the permittivity of the wafer, E_{max} is the critical electric field of the semiconductor, A is the conduction section of the drift area, V_B is the drain-source breakdown voltage of the device in off-state and μ is the drift region mobility (in an N-Mosfet $\mu = \mu_n$, with μ_n the electron mobility).

Table 1.1 shows the difference between the values of the defined quantities for both Si and SiC materials [31].

Table 1.1 Features of the Si and 4H-SiC materials [39].

	SI	**4H-SIC**
Bandgap (eV at 300°K)	1.12	3.2
Critical Electrical Field (V/cm), E_{max}	2.5×10^5	2.2×10^6
Thermal Conductivity (W/cm K at 300°K), G_{th}	1.5	$3 - 4$
Relative dielectric constant, ε_r	11.8	9.7
Electron Mobility (cm^2/V s, at 300°K), μ_n	1420	1000

As evaluated in [40], it is possible to remark that the ratio between the conduction losses through a Si and a SiC device (at $423°K$ and $600\ V$, $\mu_{n(SiC)} = 148\ cm^2/(V\ s), \mu_{n(Si)} = 576\ cm^2/(V\ s)$) where the devices are supposed to have the same conduction section A and designed for the same breakdown voltage V_B (valid just for high breakdown voltages [41]), corresponds to the ratio between the on-resistances:

$$P_{R_{on}} = R_{on} I_{rms}^2 \tag{1.2}$$

$$\frac{P_{R_{on(Si)}}}{P_{R_{on(SiC)}}} = \frac{R_{on(Si)}}{R_{on(SiC)}} \cong \frac{R_{epi(Si)}}{R_{epi(SiC)}} = \frac{\varepsilon_{r(SiC)} \mu_{n(SiC)} E_{\max(SiC)}^3}{\varepsilon_{r(Si)} \mu_{n(Si)} E_{\max(Si)}^3} = 162.69 \tag{1.3}$$

In the mentioned conditions, the SiC devices exhibit far lower conduction losses, thanks to their intrinsic features (ε_r, μ_n, E_{max}).

The mentioned features result in a remarkable improvement of the dynamical characteristics too. The dynamic behaviour of the MOSFET switching device is due to the intrinsic capacitances between the three terminals of the device, as shown in Fig. 1.12.

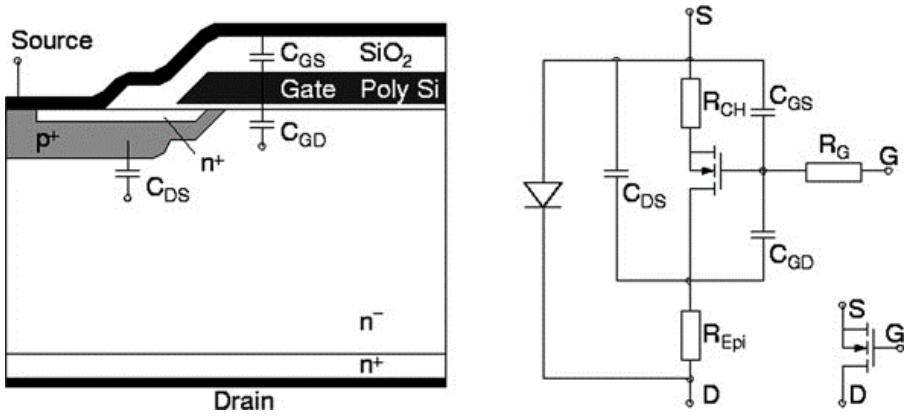


Fig. 1.12 Lumped parameter model of a MOSFET [39].

Their values determine the charging and discharging time of the gate terminal voltage, as well as of the v_{DS} voltage. It is clear that a smaller capacitances implies smaller time constants, hence shorter commutation times. The capacitance values are proportional to the section of the electrodes, hence to the dimensions of the semiconductor wafer, hence the A value. At the same on-resistance value R_{on} (i.e. same conduction losses) and the same breakdown voltage V_B, the ratio between the wafer sections A of the Si-based and SiC-based devices is given from (1.1):

$$\frac{A_{(Si)}}{A_{(SiC)}} = \frac{\varepsilon_{(SiC)}\mu_{n(SiC)}E^3_{\max(SiC)}}{\varepsilon_{(Si)}\mu_{n(Si)}E^3_{\max(Si)}} = 162.69 \tag{1.4}$$

It is clear that the SiC technology implies a great benefit in terms or dynamical behaviour too.

These features can be resumed by the specific on-resistance S of the power device, expressed as the on-resistance/area product [30]:

$$S = R_{on}A = \frac{4(V_B + V_{bi})^2}{\mu_e \varepsilon_0 \varepsilon_r E^3_{max}} \tag{1.5}$$

The S value addresses indeed the trade-off between the R_{on} conduction resistance and the cross conduction section A, hence the intrinsic capacitances values. Thus, it can be seen as a compromise between the conduction losses and switching losses of the device. The smaller the S value, the more efficient the device in term of power losses.

Another approach to compare the relative performances two different devices was introduced in [30]. It consists of a widely used figure of merit, called Baliga figure of merit, and it is defined as:

$$F_M = \varepsilon_r \mu E^3_{max} \tag{1.6}$$

The value F_M addresses the ratio between the square value of the breakdown voltage V_B and the on-resistance of the device R_{on}. The ratio between the two figures of merits results in (1.7) and confirms the superiority of the SiC technology:

$$\frac{F_{M(Si)}}{F_{M(SiC)}} = 0.0025 \tag{1.7}$$

In terms of reliability, the increase of temperature ΔT in the device due to the conduction losses is defined as:

$$\Delta T = \frac{h}{G_{th} A} P_{R_{epi}} \tag{1.8}$$

Where $G_{th}[\frac{1}{{}_{\circ}K\ m}]$ is the thermal conductivity of the semiconductor, h and A are the thickness and the cross-section of the semiconductor thermal path, respectively, and $P_{R_{epi}}$ is the wasted power.

Under the assumption of equal dimensions of the devices and equal Joule losses, the ratio between the temperature increments is equal to the inverse ratio of the thermal conductivities [40]:

$$\frac{\Delta T_{(Si)}}{\Delta T_{(SiC)}} = \frac{G_{th(SiC)}}{G_{th(Si)}} = 2.3 \tag{1.9}$$

1.3.2 Unipolar and bipolar technology: MOSFET and IGBT

For applications that requires blocking voltages higher than 1kV[1], the Si MOSFET technology exhibits some serious limitations [39]. As shown in Fig. 1.13, the current path is allowed by the enhancement of a unipolar n charge channel in the p layer beneath the gate oxide. The role of the epitaxial n^- layer, shown in Fig. 1.13, is to withstand the blocking voltage of the device during the off-state. In reverse mode, the depletion region expands through the epitaxial layer. In order to contain the electrical field in this region, the n^- region needs to be lightly doped. As a consequence, the depletion region is more extended, and the thickness of the epitaxial layer has to be increased accordingly in order to avoid avalanche phenomena in pinch-through or reach-through [38]. Briefly, the thicker the epitaxial layer, the lower the doping level and the higher the breakdown voltage.

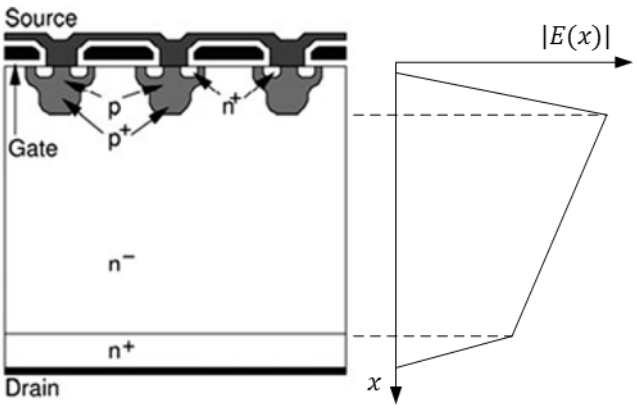


Fig. 1.13 MOSFET cross section and electric field distribution in reverse mode [39].

Nevertheless, as mentioned in the previous section, the most resistive path in a MOSFET device is the one through the epitaxial layer. A thick n^- layer lead to a high conduction resistance, hence to lower power ratings. As showed in [39], [42], the thickness w of the n layer in a p^+-n^- junction (in case of a mono-dimensional problem, i.e. infinite section A) can be expressed as:

$$w = \frac{2\ V_B}{E_{max}} = \frac{\varepsilon\ E_{max}}{q\ N_D} \tag{1.10}$$

with q as the electron electric charge and N_D as the density of donors in the n^- layer. From (1.5) and (1.10), the specific resistance S can be then expressed as:

$$S = \frac{4{V_B}^2}{\mu_e \varepsilon E_{max}^3} = \frac{4\,\varepsilon\,{V_B}^2}{\mu_e\,(q\,N_D\,w)^3} \tag{1.11}$$

where V_{bi} has been considered negligible compared to V_B. Consequently, there is always a trade-off between breakdown voltage V_B and series resistance of the device $R_{on} \cong S\,A$, which can be dealt by tuning the doping levels of the n^- and n^+ layers and the thickness of the epitaxial layer w.

These limitations lead toward the widespread of the IGBT technology [39].

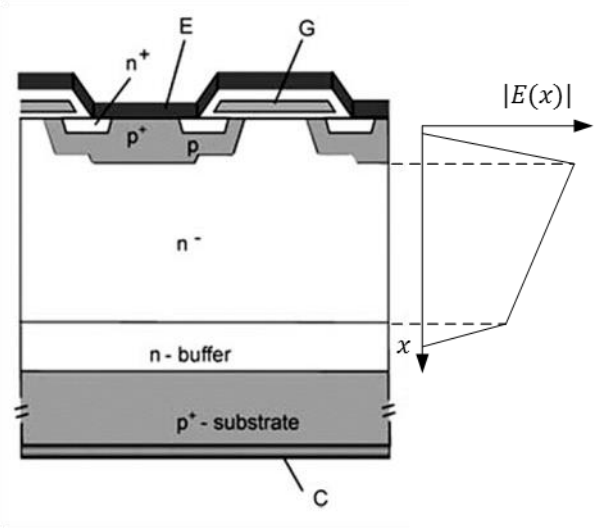


Fig. 1.14 IGBT cross section and electric field distribution in reverse mode [39].

The IGBT is a voltage controlled active switch with a structure similar to the MOSFET one, except that the IGBT has an additional p^+ region on the drain side. Consequently, an IGBT has four alternatively doped layers (p-n-p-n). IGBT current flows via the internal p-n-p transistor by turning on the internal MOSFET while voltage is applied between the collector and the emitter. It consists indeed of a bipolar minority charge carrier device. In Fig. 1.14, it is possible to recognize a typical p-i-n junction structure, which allows reducing the voltage drop through the less doped n- layer [31]. During the on-state, when the applied bias exceeds the junction built-in potential, the $p^+$and n^+ regions inject a high concentration of holes and electrons into the n- region, leading to an increase in its conductivity, hence a reduction of the resistance in the drift region. This phenomenon is called conductivity modulation. The considerably lower resistivity of the IGBT architecture compared to a silicon MOSFET allows to mitigate the trade-off conditions between the breakdown voltage and the resistance through the epitaxial layer, hence the common IGBTs off the shelf consent to reach reverse voltages of $V_{CE} > 6kV$.

On the other hand, during the transition toward the reverse mode, the great number of electrons and holes needs to be removed from the n^- layer before the formation of a depletion region can be formed to support the reverse blocking voltage, contrarily to a MOSFET device. During the turn-off, a current (called tail current) continues flowing until all the carriers accumulated by the conductivity modulation leave the drift region or disappear as a result of recombination. This phenomenon remarkably increases the turn-off time of the device and worsens its dynamic performances. Since this tail current occurs with a high V_{CE} voltage applied, it is a significant contributor to the switching power loss.

SiC technology allows to keep the dynamic performances of the unipolar devices, such as MOSFETs, and reach high operating ratings, comparable to the Si IGBTs devices. Indeed, SiC devices do not need conductivity modulation to achieve low voltage drop in conduction, since, as explained in the previous section, they exhibit a much smaller resistance through the drift-layer than Si devices. As a result, SiC MOSFETs have much lower either switching and conduction energy loss than IGBTs. This feature,

compared with Si IGBTs, enables to reach higher operating switching frequency and better efficiency. The switching frequency of Si-IGBT based converters is usually limited to 30 kHz [4]. The operating switching frequency of SiC MOSFETs based converters can reach 100 kHz in hard switching operation, which can offer a significant improvement in system compactness.

In [43] the authors carefully characterized the hard switching of an off-the-shelf SiC power MOSFET and compared it with a IGBT device with similar voltage and current ratings. A double pulse test-bed (Fig. 1.15) is set up to evaluate the devices performances in hard switched conditions.

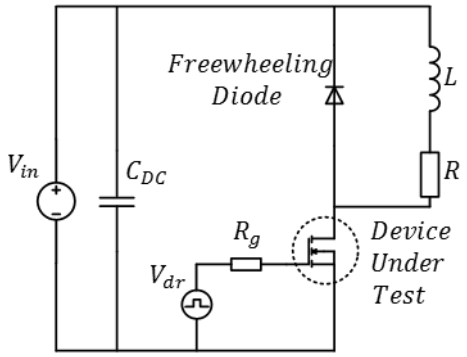
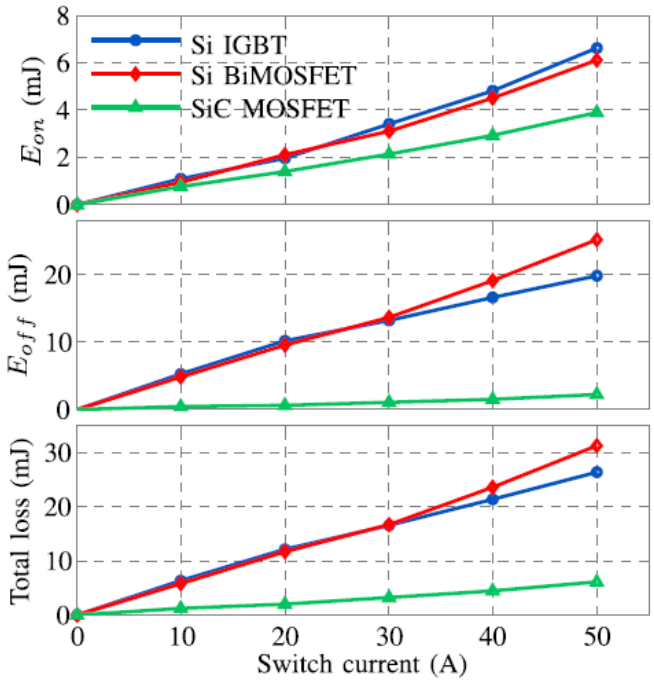


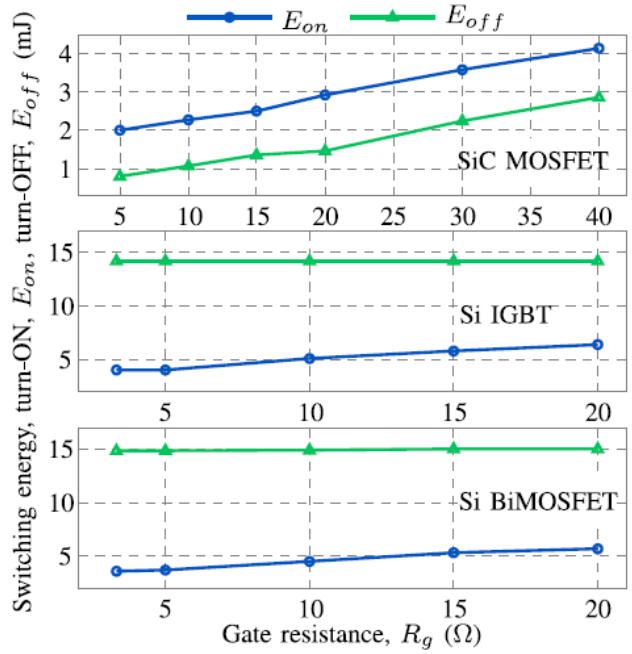
Fig. 1.15 Double pulse circuital scheme.

The power losses were evaluated in function of the gate driver resistance R_g and the conducted current I_L, with a constant DC voltage $V_{in} = 1200V$. The devices compared were the 1700-V, 50-A rated SiC MOSFET C2M0045170D produced by CREE, Inc. and a 1700-V, 32-A Si IGBT (IXGX32N170H1) produced by IXYS.

In Fig. 1.16, the SiC device performances are clearly better whatever the criteria. The switching losses increase along with both gate resistance value R_G and switching current I_L, for both devices. The only exception is the turn-off behaviour of the Si IGBT as function of the gate resistance: as expected, the energy loss mostly depends on the tail current phenomenon, which is poorly sensitive to the charging profile of the gate.



(a)



(b)

Fig. 1.16 Switching losses comparison between a SiC MOSFET C2M0045170D produced by CREE, Inc. a Si IGBT (IXGX32N170H1) and Si BiMOSFET (IXBH42N170) from IXYS, as function of the conducted current I_L ($R_g = 5\Omega$) (a) and the gate driver resistance R_g at $I_L = 40A$ (b) [43].

1.3.3 Electro-magnetic Interferences (EMI) Issues

The SiC-MOSFET unipolar components show far quicker switching times than the Si-IGBT bipolar components due to the absence of minority carriers scattered in the drift layer. But such assets do not come without any setback. Indeed, the high dv/dt and di/dt slopes are disruptive. First, they provoke

the premature ageing of electrical machines and insulators. They also increase the interaction between the driver and the power circuits due to the transfer capacitor C_{GD} of the transistor. Eventually, they disturb both the system and the surrounding electronics devices in terms of electromagnetic compatibility. In other words, they make it harder to comply with electromagnetic standards owing to the common mode current.

The SiC technology allows higher switching frequencies than Si counterpart. For instance, the selected SiC-MOSFET is able to operate up to 100kHz according to the datasheets, whereas the selected Si-IGBT is limited to the tenths of kHz [44]. However, such advantages raise issues. First, parasitic capacitors admittances and stray inductors impedances increase with frequency. Then, phenomena like LC resonant circuits and the related oscillations, or undesired coupling (capacitive and mutual), become more significant.

In order to analyse the high frequency behaviour within a switch-based power converter, idealized waveforms are frequently used to simplify the modelling of converter behaviour [45]. The switching devices are often modelled as voltage or current trapezoidal signal generators, i.e., a periodic pulse train with frequency f_s, pulse width τ , and finite rise and fall times t_r and t_f (Fig. 1.17(a)). The duty ratio D is given by $D = \tau\ /T$, where $T\ =\ 1/f_s$ is the period of the waveform. The characteristics of their spectra are widely used to understand the underlying relationships between time-domain waveform parameters and spectral content. With such approximation, the overshoots and the ringing phenomena are neglected.

Any trapezoidal signal presents a spectrum similar to the one displayed on Fig. 1.17(b). This spectrum has a bound or "envelope" which may be described (on logarithmic axes) by a series of linear asymptotes having gradients of 0 dB/dec, −20 dB/dec, and −40 dB/dec, at the corner frequencies of $1/\pi\tau$ and $1/\pi t_r$, in increasing order of frequency.

If the switching frequency increases then the spectrum is translated towards the right, i.e. up to higher frequencies. When the EMI standards are considered, it comes clear that it raises compliance problem, the standard template may not be respected.

As showed in [46]–[49], the higher transition slope of current and voltage across the device leads to a remarkable increase of the harmonic content. In [50], the double pulse test (Fig. 1.15) was performed for three combinations of the semiconductor transistor (device under test) and the free-wheeling diode, namely an all-Si combination, a Si transistor (IGBT) and a SiC-Schottky diode combination, and an all-SiC. The magnitude spectra and the envelopes of the commanded device current and voltage waveforms in the set-up of Fig. 1.15 are shown in Fig. 1.18.

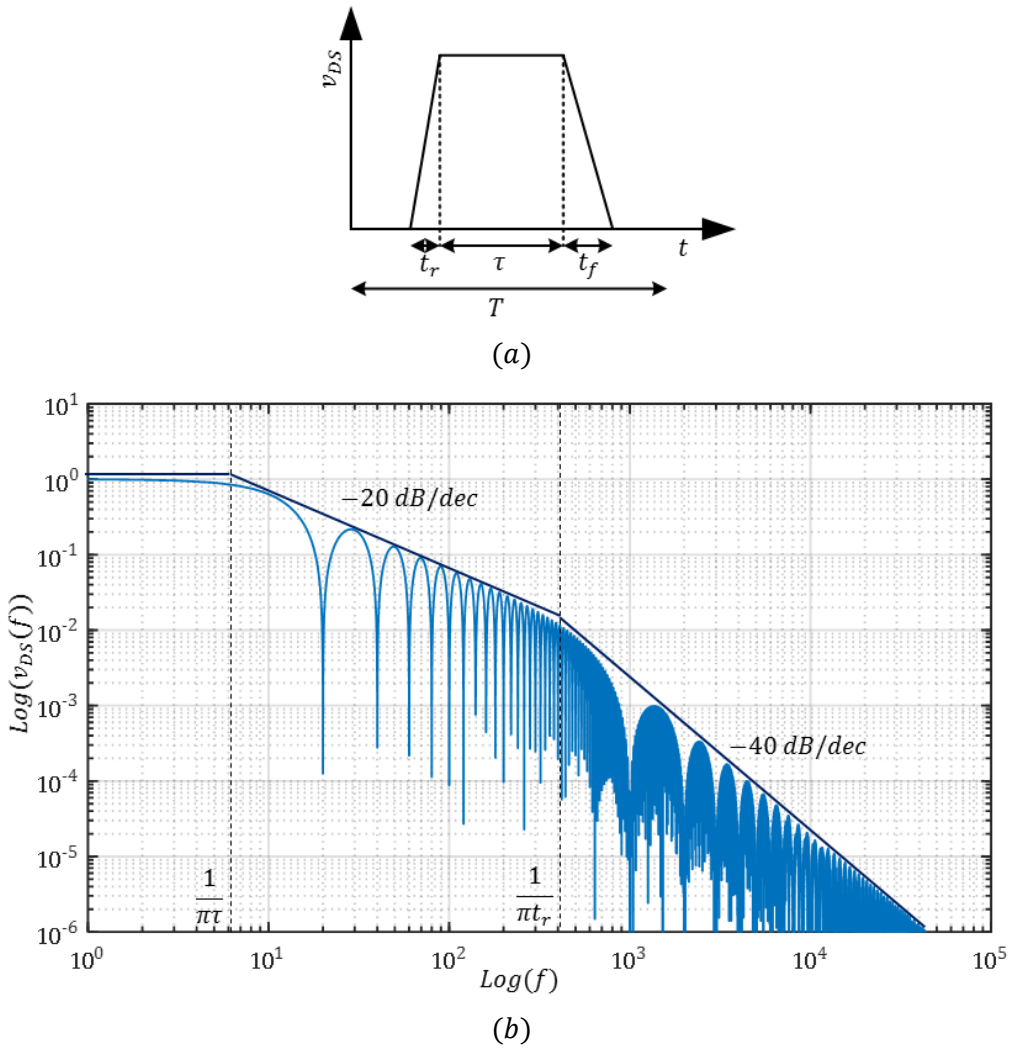
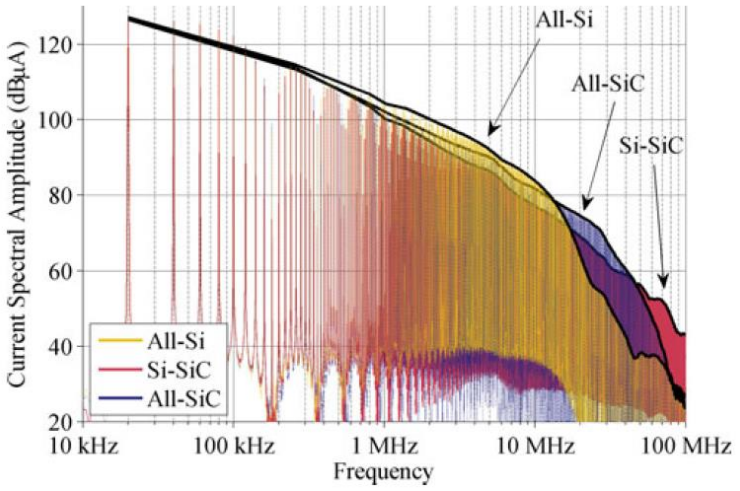


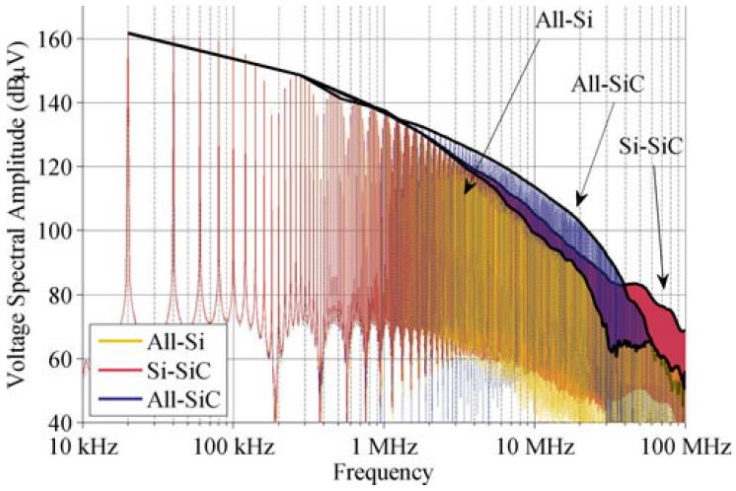
Fig. 1.17 Typical voltage trapezoidal waveform (a) common in SMPS, and its harmonic content ($t_r = t_f$) (b).

The test was performed for $V_{in} = 600\,V$, $I_L = 10\,A$, switching frequency $f_{sw} = 20\,kHz$ and a gate resistance $R_g = 27\Omega$. The tested devices were the IGBT and Si diode (Infineon IKW15T120) for all the Si configuration, a Si IGBT (IKW15T120) and SiC Schottky diode (SemiSouth SDA10S120) for the mixed configuration, SiC MOSFET (Cree CMF20120D) and SiC Schottky diode (SemiSouth SDA10S120) for the entirely SiC configuration.

The showed spectra provide an indication of the relative levels of differential-mode conducted emissions with each device combination. When a SiC diode is employed, it is possible to remark a reduction of the spectral amplitude up to 10MHz, due to the absence of diode reverse recovery. At high frequencies, the current and voltage short commutation times of the SiC devices leads to higher spectral amplitudes than the Si based configurations. At these frequencies, higher conducted emission and radiated ones as well are measured for SiC based configurations.



(a)



(b)

Fig. 1.18 Current (a) and voltage (b) spectra across the switching devices for the double pulse test performed in [50].

1.3.3.1 Si IGBT/ SiC MOSFET Experimental Comparison on a Boost converter

Prior to focusing on a specific power converter design, it is required to determine the peculiarities of the SiC MOSFET technology, not only in terms of voltage and current ratings, dynamics and static behaviours but also when it comes to implementing it in a power electronics environment. Ratings and static characteristics are generally available on the data sheet and they can be reproduced through experimental tests (output characteristic, transfer characteristic, on resistance …).

Besides the literature results provided in Fig. 1.16 and Fig. 1.18, experimental tests have been carried out at the laboratory on test benches on a boost converter. In terms of components, a Si Trench IGBT Modules SKM 195GB126D (220 A – 1200V) and a SiC-MOSFET Half-bridge Modules CREE CAS100H12AM1 (168A – 1200V) were selected mainly because of their common wide use on the market and the similar ratings. The following experimental tests are intended to verify the considerations made concerning the performances of the two devices.

In terms of converter, it is necessary to choose a circuit renowned as a reference among the power electronics community and highly widespread in the industrial field. It should be a quite simple topology so that the carried investigations can only focus on the active component behaviour and do not extend

neither to the conversion process nor to the control. Consequently, it was implemented a boost converter with the following characteristics:

- input voltage : $V_{in} = 230V$,
- output voltage: $V_{out} = 350V$,
- output power: $P_o = 3kW$.
- $L = 8.7\ mH$
- $C_o = 44$ µF

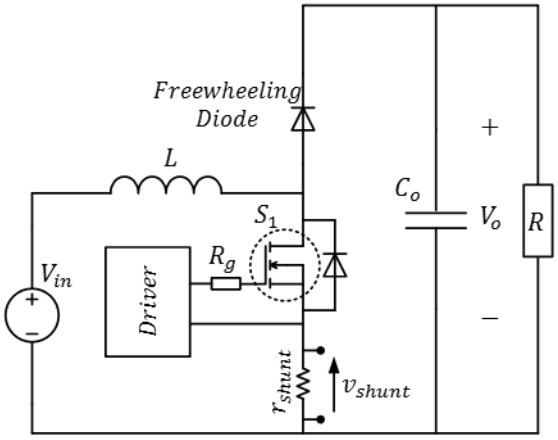


Fig. 1.19 Circuital scheme of the test bench.

The boost is asynchronously controlled, i.e. the high switch S_2 is kept open and only the antiparallel diode conducts. The load consists in a variable resistance tuned to $R = 41\Omega$ in order to have the desired output power. The operating switching frequency during the tests is $f_s = 30kHz$.

All the considered waveforms show the main values of current and voltage relative the commutation of the low switch S_1. The external driver gate resistance is $R_g = 4\Omega$ for both modules. The Boost setup does not include any snubber or additional network for the soft switching, so the commutation of the semiconductor component occurs under hard switching conditions.

The Boost is driven in asynchronous rectification mode, since the objective is to evaluate the hard-switching performance of the low switch S_1 of the modules.

1.3.3.2 Switching Behaviour

The following waveforms show the evolution of the gate voltage (v_{GE} for the IGBT, v_{GS} for the MOSFET in yellow), the emitter/source current (in light blue), the voltages (respectively v_{CE} and v_{DS}) at the device terminals (in violet) and the math function of the energy loss in orange, obtained with:

$$E_{loss} = \int_{t_0}^{t} v_{CE/DS} * i_{CE/DS}\, dt$$

Where t_0 is the initial time of the acquisition window.

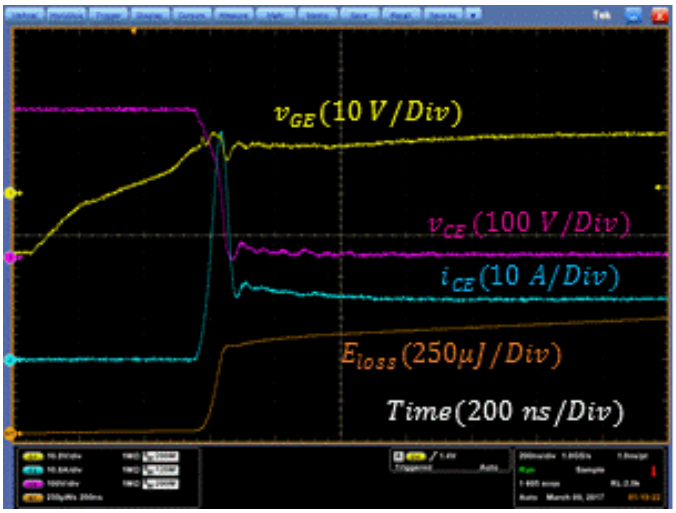
Since the commutation time of the two devices are different, especially in turn-off, the oscilloscope time division values are different in order to better observe the whole commutation, namely $t_{Div}^{IGBT} = 250\ ns$ for the IGBTs waveforms and $t_{Div}^{Mosfet} = 100\ ns$ for the SiC- MOSFET.

The devices' off-state voltages and conduction currents, referred to the waveforms in Fig. 1.20 and Fig. 1.21, are $v^{off} = V_o = 350$V and $i^{on} \cong P_o/V_{in} = 12.5$A, which represent respectively the voltage in off-state and the current in on-state.

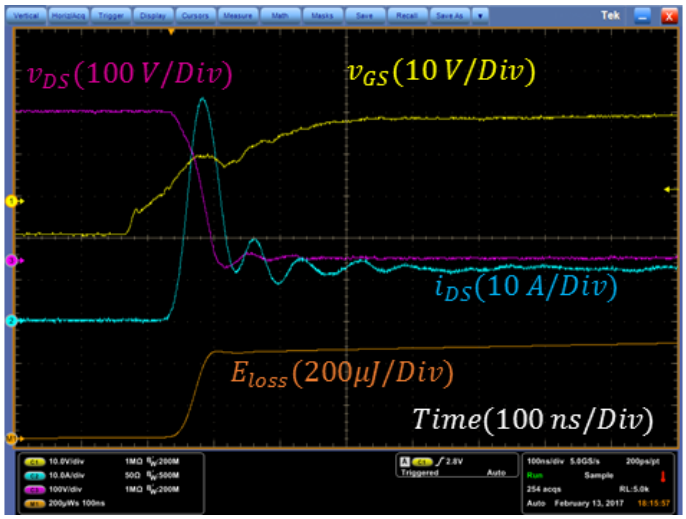
The switching times are measured by the function "*Measure*" of the Oscilloscope Tektronik DPO5054, which defines the rising and falling time between the 10% and the 90% of the waveform variation. The

slopes values (di/dt and dv/dt) are referred to the average time derivative during the commutation (from the 10% to the 90% of the conduction current value).

1.3.3.2.1 Turn on behaviour



(a)



(b)

Fig. 1.20 Turn-on waveforms for a Si-IGBT (a) and a SiC-MOSFET (b) ($V_{in} = 230V$, $V_o = 350V$, $P_o = 3kW$).

Table 1.2 Turn-on transition measurements comparison between an IGBT and a SiC-Mosfet relative to Fig. 1.20.

	$t_{rise}^{v_{GS}}[s]$	$t_{rise}^{i_{DS}/i_{CE}}[s]$	$t_{fall}^{v_{DS}/v_{CE}}[s]$	$\frac{di}{dt}[A/s]$	$\frac{dv}{dt}[V/s]$	$E_{loss}[J]$
Si-IGBT	4.41E-07	2.70E-08	6.20E-08	3.70E+08	4.51E+09	4.45E-04
SIC-MOSFET	2.45E-07	1.62E-08	4.60E-08	6.17E+08	6.08E+09	3.90E-04

The switching times and slopes relative to Fig. 1.20 are reported in Table 1.2.

The time values measured in turn-on are pretty comparable, as well as the current and voltage slopes. The rated input capacitances on the manufacturers datasheets are almost the same $C_{iss}^{(MOS)} \cong C_{ies}^{(IGBT)} \cong 10nF$.

Both the current waveforms exhibit a high over-peak of about 40 A during the turn-on. The same effect has been simulated in SABER environment: it is the result of the charge released by the discharging/charging of the intrinsic capacitors of both the switches S_1 and S_2. During the turn-on of the low device S_1, the charge stored in the intrinsic capacitor C_{oss} ($C_{oss}^{(MOS)} \cong 1nF$ for the SiC MOSFET, $C_{oes}^{(IGBT)} = 0.57nF$ for the IGBT) of S_1 is released through the resistive channel path, and an additional current flows through the channel to charge the C_{oss} capacitor of S_2, whose voltage is increases during the turn-on of the low switch. This phenomenon will be further addressed in Chapter 3 and considered in the development of the power losses model of the switching device.

Moreover, it should be remarked that, in the case of the IGBT module, the reverse recovery charge of the freewheeling diode D_2 contributes to the current peak during the S_1 IGBT turn on. In the case of the SiC MOSFET, the freewheeling diode consists of a SiC Z-Rec Diode produced by Wolfspeed, whose reverse recovery is practically absent.

The voltages and currents high frequencies oscillations after the transition are due to the interaction between the stray inductances, the parasitic capacitances between the power circuit high potential nodes and the electrical ground and the intrinsic capacitors of the semiconductor devices. Indeed, for such a fast variation of current and voltage, the impedances of these elements are no longer negligible.

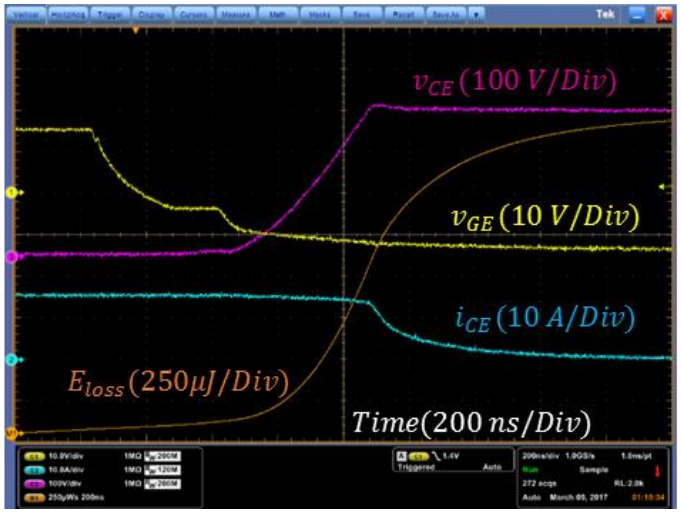
In terms of energy dissipation, the IGBT dissipation during turn-on are slightly greater than the MOSFET one (of the 14%).

It is worth remarking the differences between the energy dissipation during the conduction of the devices. Once the transition ended, the energy curves increase with different slopes. The slope of the energy wasted by the IGBT is visibly steeper than the MOSFET's one. Indeed, even if the IGBT on-resistance is smaller than the MOSFET one ($r_{CE} = 4.7m\Omega$, $r_{DS} = 16m\Omega$), the IGBT collector-emitter voltage includes the voltage drop across the active polarized p-n junction, of about $v_{CE_0} = 1.71V$.

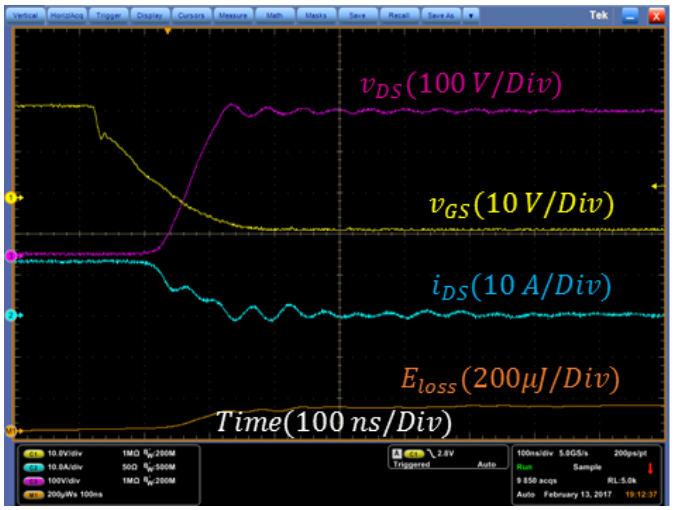
1.3.3.2.2 Turn off behaviour

The switching times and slopes relative to Fig. 1.21 are reported in Table 1.3.

The SiC device exhibits better turn-off behaviour performances. The voltage slope of the IGBT is four times slower than the SiC MOSFET one. This is a clear advantage in terms of switching losses for the SiC devices, but it also increases EMI issues. The IGBT, shows a "tail current" before it turns off totally. As already mentioned, this is a common drawback in IGBT devices, due to the evacuation of the charge left in the base of the intrinsic Bipolar-Junction-Transistor within the device. For these reasons, the turning off energy losses are considerably greater for the IGBT ($E_{loss}^{(IGBT)} \cong 16\, E_{loss}^{(MOS)}$). The turn-off behaviour can be indeed considered as the main limitation of the Si IGBT devices. The total switching losses alone amount to $E_{loss}^{(IGBT)} = 1.89 \times 10^{-3} J$ for the IGBT, compared to the $E_{loss}^{(MOS)} = 4.47 \times 10^{-4} J$ of the SiC device.



(a)



(b)

Fig. 1.21 Turn-off waveforms for an IGBT (a) and a SiC- MOSFET (b) ($V_{in} = 230V$,$V_o = 350V$, $P_o = 3kW$).

Table 1.3 Turn-off transition measurements comparison between an IGBT and a SiC-Mosfet relative to Fig. 1.21.

	$t_{fall}^{v_{GS}}[s]$	$t_{fall}^{i_{DS}/i_{CE}}[s]$	$t_{rise}^{v_{DS}/v_{CE}}[s]$	$\frac{di}{dt}[A/s]$	$\frac{dv}{dt}[V/s]$	$E_{loss}[J]$
Si-IGBT	4.90E-07	2.48E-07	3.07E-07	4.03E+07	9.12E+08	1.45E-03
SIC-Mosfet	1.77E-07	1.01E-07	7.50E-08	9.90E+07	3.73E+09	8.70E-05

1.4 Conclusion

In this chapter, it has been provided a general introduction to the context and the application domain in which the thesis subject belongs. The recent trend toward efficiency and autonomy in the transportation sectors, make MEA and HEV/EV an interesting research subject. Due to the progressing substitution of mechanical parts by electrically powered ones and the increase of the electrical power needed by minor loads, the power handled by the on-board electrical network is constantly increasing. A DC interface between the generation block and the several loads of the grids is currently largely employed in the micro-grid structure for embedded applications. Each power load needs to be adapted to the DC bus through an opportune converter, whose role is to provide the demanded power and voltage according to the load requirements and the application standards (current and voltage harmonic content on the bus). Moreover, it shall protect both load and DC network from possible voltage and power disturbances and variations on both sides (voltage response to power variations), which could compromise the reliability of the system. The employ of HVDC micro-grids brings several advantages to the performances of the switched power converters on-board, mostly for the electrical traction and the storage energy systems.

In parallel, these SMPS for on-board applications remarkably benefited from the development of WBG devices, which contributed to reach new levels of efficiency and compactness. The WBG allow to build unipolar devices with blocking voltages similar to the IGBTs ones. For the same blocking voltage, the conduction resistance of WBG MOSFETs is very low compared to the IGBT, which allow to reduce the area of the conduction section, with a consequent improvement of the dynamic performances. The switching behaviour is further improved due to the absence of restoring charge phenomena, typical of bipolar devices. SiC MOSFETs are technologically mature to replace the classical Si IGBT used for this kind of applications, as showed by experimental validation performed in several study and during the thesis work.

2 DC/DC Power Conversion in an Embedded Powertrain Application

2.1 Introduction

As showed in the last chapter, each load connected to the embedded DC network needs to be adapted through an opportune conversion chain, which should both provide the required voltage and power to the load and comply with the application standards concerning the conducted interferences on the network. The subject of this study is a DC/DC power converter, which may constitute a part of a more global chain of actuators, a starter application for instance. The classical architecture of the power electronics stage in a motor drive application usually consists of an input filter, a Voltage Source Inverter (VSI) and a motor. For both EV/HEV and aeronautics environments, it has been showed that the interposition of a DC/DC converter between the input filter and inverter allows to optimize the power electronics stage [51]–[55]. The insertion of the extra converter allows adding another degree of freedom on the input voltage of the inverter, with several benefit on the size, cost and power losses of the actuator assembly. In this chapter, the particular case of the MEA application is treated, where the wide variation of the DC bus voltage makes the mentioned solution even more interesting.

In the first part of the chapter, the most common DC/DC converter topologies for a powertrain application are presented. According to the speed/torque requirements along an entire mission cycle, the best solution could be represented by a step-up or a step-up/down DC/DC converter topologies. The first ones are preferred when the mission cycle requires mostly a high mechanical speed. When a high speed is demanded for just a small portion of the mission cycle period, a step-up/down topology could be a better choice.

Besides the classical topologies, the Z-Source (Impedance Source) converter topologies recently gained a considerable success in motor drive applications [56]. In the last part, a new DC/DC step-up/down topology has been proposed specifically for a starter motor drive application. The proposed converter is a modified version of a Quasi Z-Source converter [57]. The operating principles and the most convenient command strategy (in terms of power losses) have been described. An experimental prototype has been realized and tested to show the feasibility of the proposed solution. Finally, the proposed topology has been compared with a SEPIC converter, a common step-up/down topology with similar features.

2.2 DC/DC power converters for Starter applications in a MEA

As already discussed in the first chapter, in the particular case of the MEA, Variable Speed Generators are used to suppress the mechanical gearboxes in order to increase the reliability of the high power sources. The AC network voltage of these aircrafts and consequently the voltage level of the different DC-buses may vary considerably. The secondary loads are supplied through a DC bus obtained by the rectification, through an Auto-Transformer Rectification Unit (ATRU), of the variable frequency/amplitude AC voltage generated by the Variable Speed Generator (VSG) through an uncontrolled rectifier unit. The voltage value of the DC bus with a nominal voltage of 270V can indeed vary from 230V to 335V. Furthermore, the electrical loads need to be connected through an input filter

in order to decouple each load form the other and to comply with the aeronautical EMC standards for conducted disturbances that may occur on DC bus.

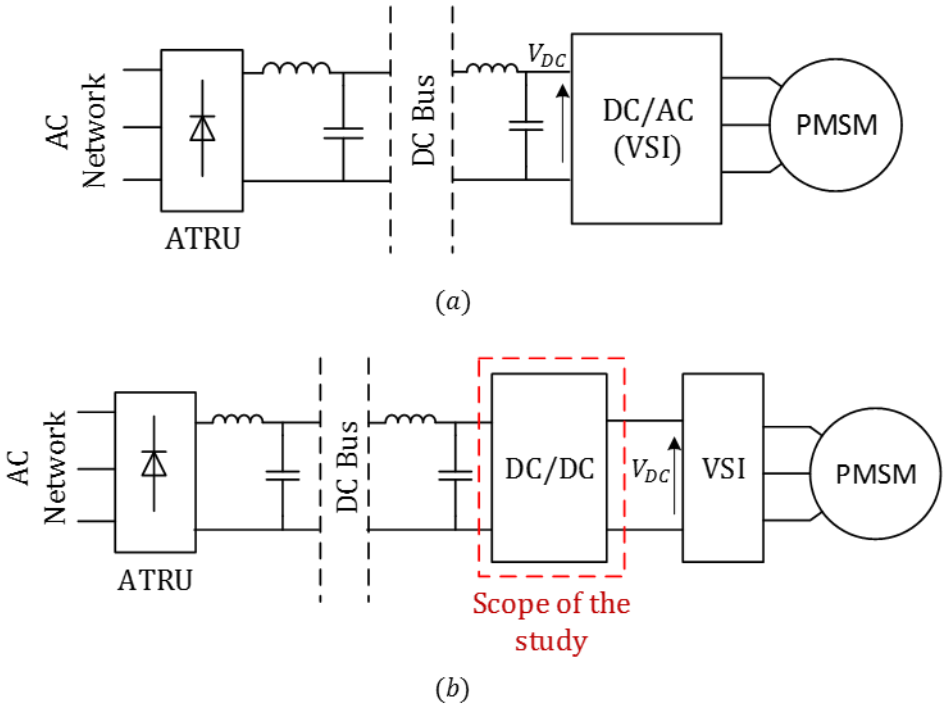


Fig. 2.1 Classical conversion chain (a) for a motor drive power supply and with a DC/DC converter between the DC Bus and the inverter (b).

In recent years, the advancements in permanent magnet technologies, fault tolerant design and high performance control [58]–[60] made the Permanent Magnet Synchronous Motor (PMSM) a popular candidate for the realization of electromechanical actuators. Fig. 2.1(a) shows the basic set up of a PMSM actuator connected to the micro-grid only through an LC filter and a VSI.

When connected to a DC bus with variable voltage, especially when the DC voltage assumes a low value, the increase of the back electromotive force inducted in the windings of the motor phases at the maximal speed could lead to the inability to control the stator phase currents [61], [62]. The number of coils of the windings shall be then accordingly reduced, which lead to higher phase currents for a given value of mechanical torque. A lower number of coils practically does not impact the power losses and the inducted magnetic field within the motor stator itself, rather it affects the ratings, the size and the power losses of the VSI. The ratings of the switching devices of the inverter shall be chosen for the worst cases. As for the current rating, the VSI provides its maximum current when the DC bus voltage is the lowest and the required torque is the maximal. As for the voltage rating, the maximum sustain voltage by the semiconductors occur for the highest value of the DC bus voltage. The switching devices will then result oversized, which leads to higher costs. Furthermore, for a lower number of coils and a given value of torque, the VSI should provide higher phase currents, then the heatsink shall be oversized in order to face the higher power losses through the switches.

In order to avoid these drawbacks, an extra DC/DC converter can be added between the input filter and the VSI supplying the PMSM [59], [60], as it is shown in Fig. 2.1(b).

In the following sections, the most classical topologies of DC/DC converter will be presented, based on the application requirements. The topologies are presented in their bidirectional version, since regenerative braking, battery charging and backup power are often required in such applications.

The considered converters are non-isolated, since the isolation is achieved through bulky magnetic elements that considerably worsen the compactness and the weight of the converter, which is of primary

importance in embedded systems. Moreover, for a powertrain application the isolation feature of the ground potential is not necessarily required, even if it could remarkably improve electromagnetic compatibility related issues [63], [64].

2.2.1 DC/DC Step-up converters topologies

The reachable speed of the PMSM is proportional to the maximal available phase voltage magnitude, i.e. the DC voltage upstream the VSI (V_{DC} in Fig. 2.1(b)). The maximal voltage is determined by the available V_{DC} value and the modulation method. In order to extend the range of speed, a traditional flux weakening method could be applied [65], [66], which can be realized by applying a demagnetizing d-current in the dq frame. However, this method increases the winding copper losses and also risks irreversible demagnetization of the machine core.

In terms of losses, it is preferable to adapt V_{DC} to the maximal speed within the application mission profile. When a high speed is required for the most part of the operating cycle, a step-up DC/DC converter is often employed. The classical step-up architectures are presented in the following subsections.

2.2.1.1 Boost converter

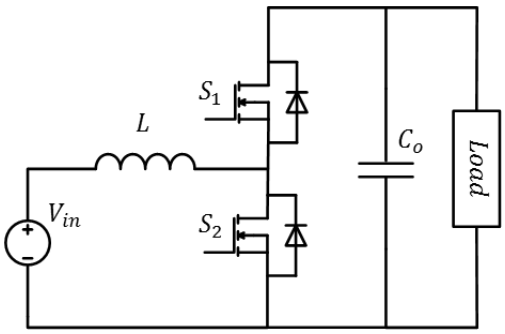


Fig. 2.2 DC/DC Boost converter.

The most common step-up converter is surely the Boost converter (Fig. 2.2), largely employed for its simplicity, minimum component count and reliability. The series connected inductor L with the input DC source helps reducing the input current ripple and a capacitor at the output side eliminates the output voltage ripple. The output capacitor should be chosen large enough to contain the discontinuous current.

Among its main features, a moderate output voltage gain can be obtained (usually <4) and the input current is continuous, which leads to a small input filter to meet the EMI requirements. Other advantages of this topology include easy and reliable operation principle, cost effectiveness, and high efficiency in both directions, which makes it a suitable option for EV/HEV and MEA powertrains [4], [28], [67].

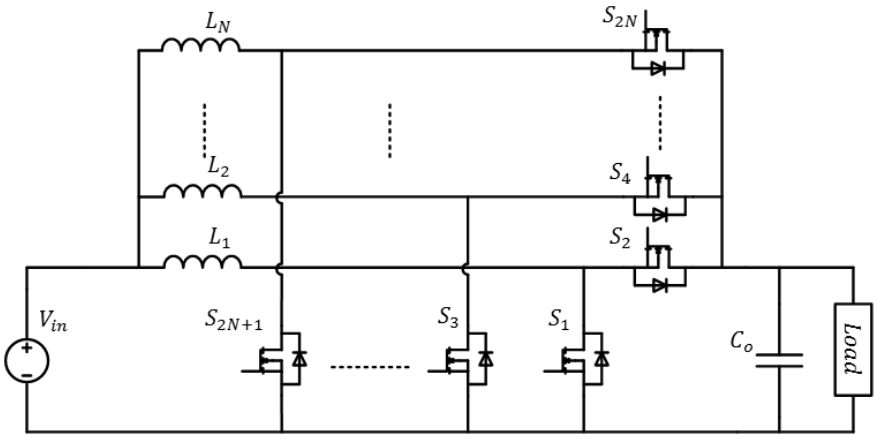


Fig. 2.3 Interleaved Boost converter.

The interleaved version of the boost converter, shown in Fig. 2.3, can attain a higher voltage gain thanks to the consistent reduction of the power losses. Indeed, even if the higher number of components increases the cost and the complexity of the command signals generation, the lower conducted current by each switch improves the conversion efficiency. Although the greater number of cores (in case of magnetically uncoupled structure), the input current is shared between the inductors and the overall stored magnetic energy is lower than in the single leg boost converter. Moreover, the weight of the magnetic core could be further reduced by coupling the inductors. The input filter and the output capacitor sizes results reduced as well, since the fundamental frequency of the input and output current waveforms is equal to the switching frequency multiplied for the number of legs [68], [69]. If opportunely designed, the interleaved structure offers the possibility of reducing the overall size of the assembly converter/input filter.

2.2.1.2 Z-Source Converter

The first studies about impedance fed converters date back to 2003. In [56], a new topology of DC/AC inverter was described, shown in Fig. 2.4, for electrical traction which introduces the possibility to step up and down the AC output voltage amplitude by only commanding the inverter switches.

The traditional three-phase VSI has six active configurations and two zero states, where the load terminals are shorted through either the lower or upper three devices, respectively.

The three-phase Z-Source inverter, composed by the assembly of the Z-Source converter and the inverter, is featured by an additional configuration, called shoot-through, which occurs during the zero-state configurations, where one or more legs of the inverter are shorted out and $V_{DC} = 0$. The d_{cc} duty cycle of the shoot-through determines the boosting factor of the V_{DC} voltage:

$$\frac{V_{DC}}{V_{in}} = \frac{1}{1 - 2d_{cc}} \tag{2.12}$$

A visible disadvantage of this topology comes from the presence of the diode at the input terminal. Because of the input discontinuous input current, the input filter shall provide a bigger attenuation of the harmonic content at the switching frequency to comply with the application standards, which leads to a bigger size.

The same authors, in a successive work [57], showed some evolutions of the original Z-Source inverter topology, which solve several problems like the input current discontinuity or the excessive voltage/current stress through the converter passive elements. For the considered application, the voltage fed Quasi Z Source Inverter (QZSI) shown in Fig. 2.5 is particularly suited.

The operating principles of the QZSI are pretty the same, with the same voltage gain expressed in (2.12). On the other hand, this topology is featured by a continuous input current because of the L_1

inductor. As it will be shown in Section 2.3.2, with an opportune coupling of the two inductors it is possible to totally suppress the current ripple at the switching frequency, with a consistent gain on the size of the input filter [70].

Due to the shoot-through state, this topology is unsuitable for the generation of the inverter switches command signals through a Pulse Amplitude Modulation (PAM), which is an interesting alternative to the Pulse Width Modulation (PWM) [62]. The PAM could bring several benefits to the overall system performances, especially at high speeds. Such strategy allows indeed to considerably reduce the switching occurrences of the inverter transistors, with a consequent reduction of the power losses. Moreover, it enables to reduce the high frequency harmonic content conducted in the network which could be harmful for the stator windings and increase the voltage gain on the AC side.

A possible solution to overcome such limitation consists in the topology proposed in Fig. 2.6, where the power load (inverter/PMSM) is connected to the C_1 converter, as in [71].

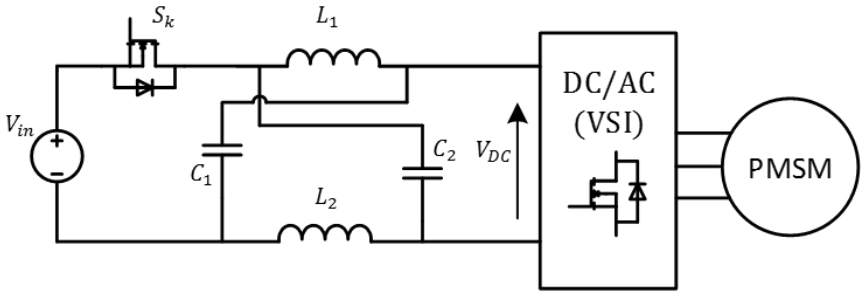


Fig. 2.4 Z-Source Inverter.

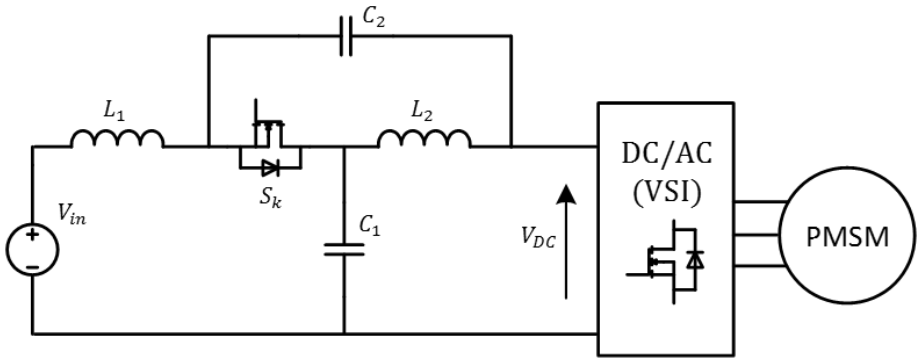


Fig. 2.5 Quasi Z-Source Inverter.

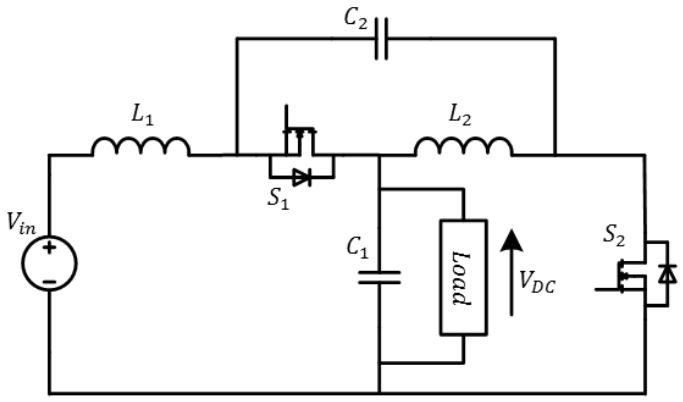


Fig. 2.6 Alternative version of Quasi Z-Source converter [71].

2.2.2 DC/DC Step-up/down converters topologies

When the actuator is composed by a step-up converter and the inverter, if a low mechanical speed is required, the amplitude of the motor phases AC voltage is achieved by lowering the inverter PWM modulation index. Anyway, the high voltage stress on the inverter switches and the recurrent commutations could remarkably decrease the efficiency of the inverter.

The addition of a DC/DC converter in the power chain of actuators is also proposed in [72], [73] by applying a PAM control, which permits to reduce the VSI losses and to improve the actuators performances at high speeds.

In case of constant DC-bus voltage, the PMSM has to be designed according to its speed limit in order to ensure the current controllability of the motor at the DC-bus voltage. In applications like starters, the used actuators equipped with PMSM operate at low speeds in major part of the mission cycle and at higher speeds occasionally during a short interval [51], [74]. At low speeds, a DC inverter input voltage lower than the input DC-bus voltage is required. At higher speeds, the inverter input voltage should be increased; hence the bus voltage boosting is required. The operating cycle can be assumed similar to the one shown in Fig. 2.7, during which a boost conversion is required in a short interval of the working cycle period T_{cycle}.

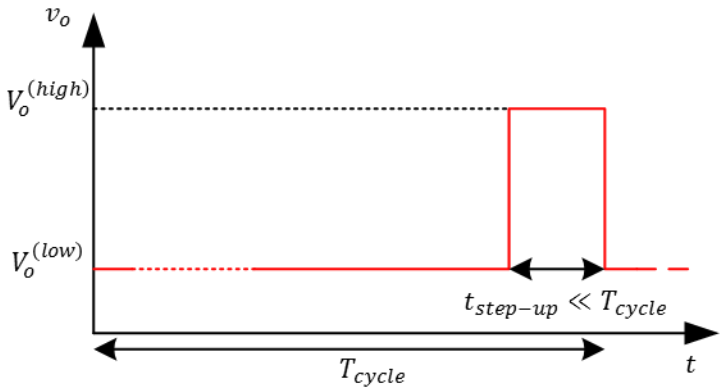


Fig. 2.7 V_{DC} typical operating cycle of a wide range speed application.

The VSI and the motor windings should be designed to ensure the controllability of the phase currents in the whole range of mechanical speed. If the V_{DC} voltage is kept at low values, for example through a step-down DC/DC converter, it is necessary to design the PMSM with a low phase turns number to reach the maximal speed with the available DC-bus voltage. It means that, during the main part of the mission cycle at low speeds, the PMSM works with a lower inverter input voltage and a high phase motor current. Therefore it is necessary to over-size the current range of the VSI only for a negligible part of the mission cycle.

An optimal trade-off can be achieved by using a step-up/down DC/DC stage feeding the inverter, instead of a step-up converter [73], [75]. Thus, it is possible to realize the PAM control strategy on practically the entire speed range, so to improve the VSI efficiency and the system compactness as well.

2.2.2.1 Buck-Boost Converter

The first presented topology is a Buck-Boost converter, a non-inverting structure renowned for its simplicity, high reliability and relatively few semiconductors, with voltage gain:

$$\frac{V_o}{V_{in}} = \frac{d}{1-d} \tag{2.1}$$

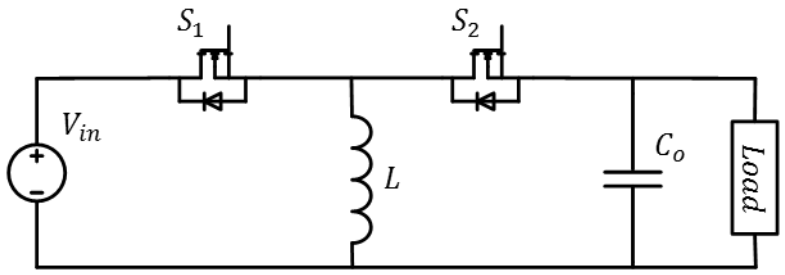


Fig. 2.8 Buck-Boost converter.

Nevertheless, the input current is discontinuous because of the switching device, which implies the requirement of a high attenuation at the switching frequency harmonic, then a bulky input filter. Furthermore, because of the discontinuous current upstream the output capacitor, the output capacitance shall be oversized to keep the output voltage within the voltage ripple requirements.

2.2.2.2 CUK converter

The Cuk converter (named after Slobodan Cuk) is an inverting DC-DC topology, showed in Fig. 2.9. Both input and output currents are inductive, hence continuous. This feature makes easier the filtering of the input and output voltages. The C_1 capacitor decouples the input and output power stages, but it conducts a high RMS current and sustain a high voltage ($V_{C_1} = V_o + V_{in}$). The voltage gain is given by (2.1), where d represents the duty cycle of the switch S_1.

It consists of 4 passive elements, which makes the study of the dynamical behaviour pretty challenging. Further issues concerning the control are caused by the right-half plane zero, since it is a boost derived topology.

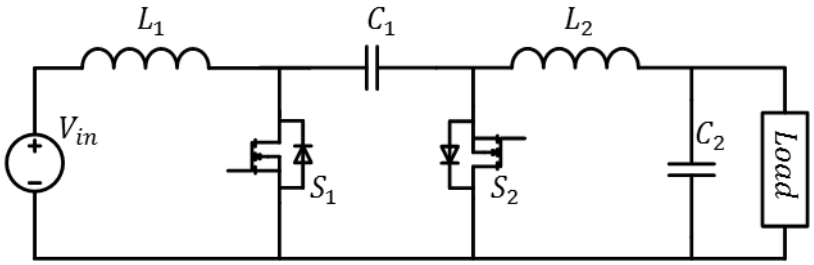


Fig. 2.9 CUK converter.

2.2.2.3 SEPIC converter

The Single-Ended Primary Inductance Converter (SEPIC), shown in Fig. 2.10, is a non-inverting topology. The capacitor C_1 isolates the input from the output and provides protection against a shorted load. The output current is discontinuous, indeed it requires to be filtered by a large capacitor C_2. As for the Cuk converter, the voltage gain is given by (2.1).

As the CUK converter, it is a 4^{th} order boost derived topology, hence it raises additional control issues.

Another classical step-up/down topology is the Z converter, shown in Fig. 2.11. It consists of a 4th order non-inverting architecture, with the same voltage gain as in (2.1), where d represents the duty cycle of S_1 in Fig. 2.11. This topology is very similar to the CUK and SEPIC converters, with the advantage that it does not suffer from the right-half plane zero issue. As for the SEPIC, the voltage of the decoupling capacitor C_1 is $V_{C_1} = V_{in}$, and the output capacitance C_2 can be considerably low, because of the presence of the inductor L_2 which provides a continuous current. Nevertheless, the input filter, as for the buck-boost case, shall be oversized to provide a high attenuation to the input current harmonic at the switching frequency.

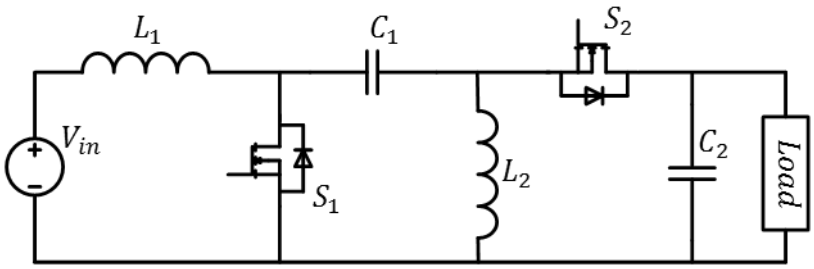


Fig. 2.10 SEPIC converter.

2.2.2.4 Z Converter

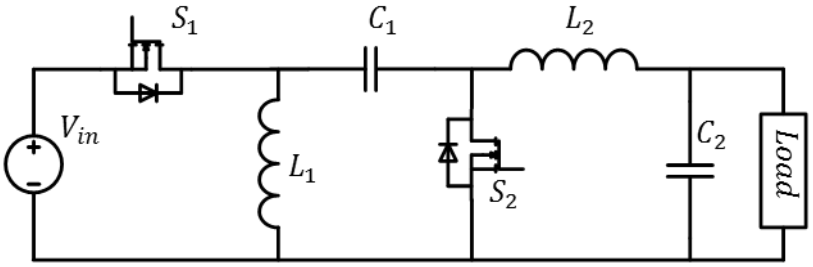


Fig. 2.11 Zeta converter.

2.3 Proposed QZS step up/down DC/DC converter topology and its modelling

In the context of a motor drive application, presented in Section 2.2.2, a new DC/DC step-up/down converter based on a QZS structure is presented [71]. The proposed topology is composed of a Quasi Z-Source network and a buck converter downstream as shown in Fig. 2.12 (it will be referred as QZSBC in this document).

The converter is conceived for a starter power supply of a PMSM for an on-board More Electric Aircraft application, specifically through a PAM inverter. As mentioned, the mission cycle of a starter requires a low mechanic speed for the most part of the time. It has been already remarked that, when the actuator is composed by a classical VSI, the upper speed is limited by the DC bus voltage. Furthermore, when it is required a low mechanical speed, the difference between the DC bus voltage and the electromagnetic force induced on the stator windings cause a high ripple of the phase currents, then of the torque. Such distortion deteriorates the speed control performances.

The actuator composed by a DC/DC step-up/down converter and PAM inverter can solve both issues.

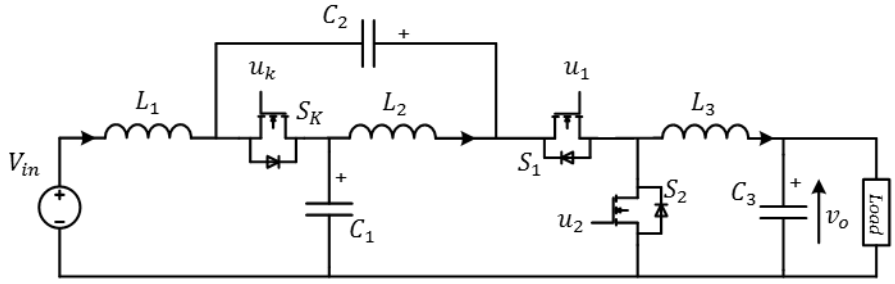


Fig. 2.12 Proposed Quasi Z-Source step up/down DC/DC converter topology.

Furthermore, to satisfy the aeronautic standards DO-160, the DC/DC converter input current needs to be filtered in order to avoid electromagnetic interference effects into the network. A usual approach to overcome this issue is to use bulky *LC* input filters that increase the cost, the power losses and the volume of the system. In literature several techniques for the total suppression of the input current ripple have been considered. They usually involve the use of additional components and active filters [76], [77].

Among the most renowned existing step-up/down non-isolated converters, the CUK and SEPIC structures exhibit an input current smoothed by its inductors, which allows the reduction of the size of the input filter. Moreover, the input current ripple can be almost suppressed by an appropriate coupling of their inductors [70]. In this way, the weight and the cost of the input filter shown can be considerably reduced. As it will be shown, the proposed DC/DC step-up/down QZS converter presents indeed the possibility to suppress the input current ripple through magnetic coupling means.

In Section 2.3.4, a comparison is conducted among the proposed converter and a SEPIC because of the common features, as non-inverting output voltage and smooth input current. The results of the comparison (Section 2.3.4) show that, for a voltage gain within [0.5;1.5], the QZSBC topology exhibits a lower stress on the active components and lower value of magnetic and static energy stored by the passive components, which makes it an interesting topology in terms of compactness.

2.3.1 Operating principles

In the following analysis, a binary variable u_i specifies the logic state of the generic switch i: when $u_i = 1$ the switch i is turned on and when $u_i = 0$ the switch is turned off. The configuration of the circuit is managed by the state of the two active switches of the buck converter side u_1 and u_2. The command signal of the switch S_K depends on u_1 and u_2 and is set to $u_K = \overline{u_1.u_2}$. It should be noted that the command signals u_1 and u_2 are never simultaneously zero. Therefore only three sequences can be envisaged. It is possible to admit either the simultaneous on-state of both buck active switches ($u_1 = u_2 = 1$) or the on-state of only one of them ($u_1 = 1$ and $u_2 = 0$, or $u_1 = 0$ and $u_2 = 1$).

In this first approach the inductors L_1 and L_2 are assumed to be uncoupled magnetically. For ease of discussion, the case of a resistive load R has been considered.

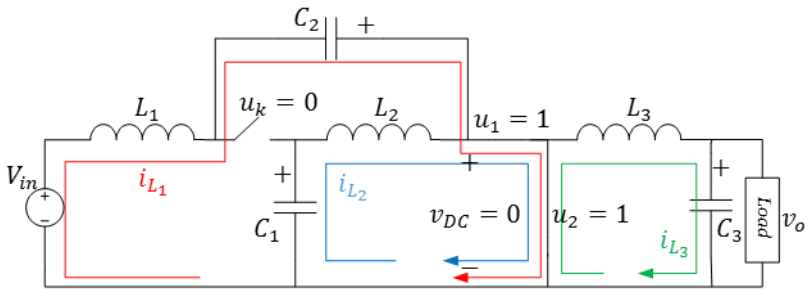


Fig. 2.13 QZSBC configuration in Shoot-Through Mode ($u_1 = u_2 = 1, u_K = \overline{(u_1.u_2)} = 0$).

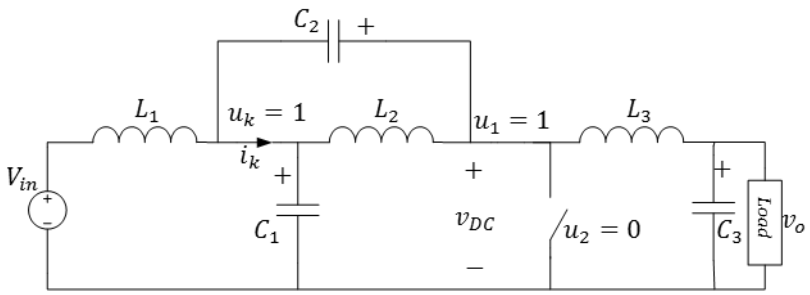


Fig. 2.14 QZSBC configuration during Conduction Mode ($u_1 = 1,\ u_2 = 0, u_K = \overline{(u_1.u_2)} = 1$).

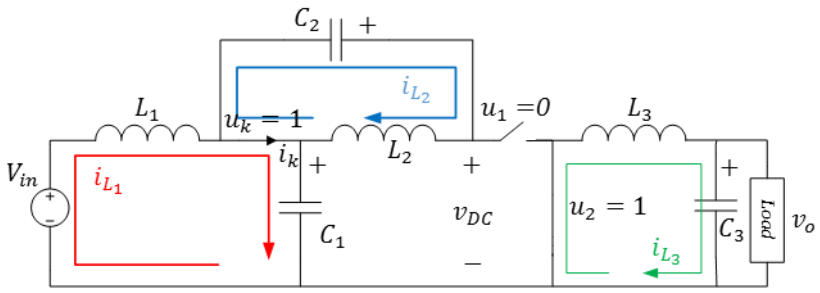


Fig. 2.15 QZSBC configuration during Open Circuit Mode ($u_1 = 0, u_2 = 1, u_K = \overline{(u_1.u_2)} = 1$).

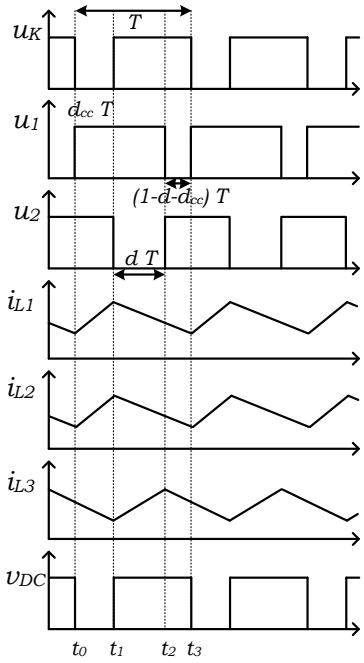


Fig. 2.16 Time evolution of QZSBC switches logic states, inductors currents and v_{DC}.

Fig. 2.16 shows the theoretical waveforms of the main electrical and logical quantities of the circuit during a switching period T_s. The following three operating configurations can be considered, namely:

- ***Shoot-Through Mode, $t \in [t_0, t_1]$:*** both switches of the Buck side, u_1 and u_2 are on simultaneously ($u_1 = u_2 = 1$), hence the switch K is off ($u_K = 0$). The QZSBC configuration in this mode is shown in Fig. 2.13. The duration of this mode is $t_{cc} = d_{cc}\, T_s = (t_1 - t_0)$ (Fig. 2.13), the shoot-through duty ratio is defined by $d_{cc} =< u_1 u_2 >_{T_s} = t_{cc}/T_s < 1$.
- ***Conduction Mode, $t \in [t_1, t_2]$:*** the top buck switch u_1 is on and the bottom one is off ($u_1 = 1$ and $u_2 = 0$), hence the switch K is on ($u_K = 1$). The QZSBC topology is configured as shown in Fig. 2.14. The duration of this mode is $t_{conduction} = d\, T_s = (t_2 - t_1)$, the conduction mode duty ratio d is then defined by $d =< u_1.\overline{u_2} >_{T_s} = t_{conduction}/T_s < 1$.
- ***Open Circuit Mode, $t \in [t_2, t_3]$:*** the top buck switch u_1 is off and the bottom one is on ($u_1 = 0$ and $u_2 = 1$), hence the switch K is on ($u_K = 1$). The QZSBC is configured as shown in Fig. 2.15. The duration of this mode is $t_{open-circuit} = (1 - d - d_{cc})T$. In this mode, the QZS side and the buck side of the converter shown in Fig. 2.15 have no power exchange ($u_1 = 0$).

The behaviour of the proposed QZSBC during the three mentioned configurations can be represented by a single mathematical dynamic model using the Boolean variables u_1 and u_2, knowing that u_K is obtained from u_1 and u_2 ($u_K = \overline{u_1.u_2}$):

$$\begin{cases} L_1 \dfrac{di_{L_1}}{dt} = u_1 u_2 (V_{in} + v_{C_2}) + u_1 \overline{u_2} (V_{in} - v_{C_1}) + u_2 \, \overline{u_1} (V_{in} - v_{C_1}) \\ L_2 \dfrac{di_{L_2}}{dt} = u_1 u_2 (v_{C_1}) + u_1 \overline{u_2} (-v_{C_2}) + u_2 \overline{u_1} (-v_{C_2}) \\ C_1 \dfrac{dv_{C_1}}{dt} = u_1 u_2 (-i_{L_2}) + u_1 \overline{u_2} (i_{L_1} - i_{L_3}) + u_2 \overline{u_1} i_{L_1} \\ C_2 \dfrac{dv_{C_2}}{dt} = u_1 u_2 (-i_{L_1}) + u_1 \overline{u_2} (i_{L_2} - i_{L_3}) + u_2 \overline{u_1} i_{L_2} \\ L_3 \dfrac{di_{L_3}}{dt} = u_1 u_2 (-v_{C_3}) + u_1 \overline{u_2} (v_{C_1} + v_{C_2} - v_{C_3}) + u_2 \overline{u_1} (-v_{C_3}) \\ C_3 \dfrac{dv_{C_3}}{dt} = i_{L_3} - \dfrac{v_{C_3}}{R} \end{cases} \quad (2.2)$$

Then:

$$\begin{cases} v_{DC} = \overline{u_1 . u_2} \, (v_{C_1} + v_{C_2}) \\ i_K = u_1 \overline{u_2} (i_{L_1} + i_{L_2} - i_3) + u_2 \overline{u_1} (i_{L_1} + i_{L_2}) \end{cases} \quad (2.3)$$

During the *shoot-through mode* ($u_1 = u_2 = 1$), the reverse voltage across the switch K is negative ($V_K = -v_{C_1} - v_{C_2} < 0$ and $i_K = 0$, Fig. 2.13) and $v_{DC} = 0$. The voltages across the inductors L_1 and L_2 are positive and their currents (i_{L_1} and i_{L_2}) increase (Fig. 2.16). In the same time, the currents of the capacitors C_1 and C_2 are negative and the voltages across them (v_{C_1} and v_{C_2}) decrease. During the *conduction mode* ($u_1 = 1$ and $u_2 = 0$), the current in switch K ($i_K = i_{L_1} + i_{L_2} - i_3$) can be positive or negative. Since $v_{DC} = v_{C_1} + v_{C_2} > v_{C_3}$, the inductor L_3 is charging. The other inductors (L_1 and L_2) start to discharge. In *open circuit mode* ($u_1 = 0$ and $u_2 = 1$), the inductor L_3 stays in discharging phase, meanwhile the currents i_{L_1} and i_{L_2} are obtained from the equations of the state variables given in (1). During this mode the current in switch K is positive ($i_K = i_{L_1} + i_{L_2} > 0$) and $v_{DC} = v_{C1} + v_{C2} > 0$.

Considering that $d_{cc} =< u_1 u_2 >_T$, $d =< u_1 \overline{u_2} >_T$ and $(1 - d - d_{cc}) =< u_2 \overline{u_1} >_T$, the dynamical average model of the QZSBC can be deduced from the instantaneous time model in (2.2):

$$\begin{cases} L_1 \dfrac{di_{L_1}}{dt} = d_{cc}(v_{C_2}) - (1 - d_{cc}) v_{C_1} + V_{in} \\ L_2 \dfrac{di_{L_2}}{dt} = d_{cc}(v_{C_1}) - (1 - d_{cc}) v_{C_2} \\ C_1 \dfrac{dv_{C_1}}{dt} = d_{cc}(-i_{L_2}) - d(i_{L_3}) + (1 - d_{cc}) i_{L_1} \\ C_2 \dfrac{dv_{C_2}}{dt} = -d_{cc}(i_{L_1}) - d(i_{L_3}) + (1 - d_{cc}) i_{L_2} \\ L_3 \dfrac{di_{L_3}}{dt} = d(v_{C_1} + v_{C_2}) - v_{C_3} \\ C_3 \dfrac{dv_{C_3}}{dt} = i_{L_3} - \dfrac{v_{C_3}}{R} \end{cases} \quad (2.4)$$

Using the dynamic average model (2.4), it is possible to determine the state variables mean values in steady state as functions of the duty cycles d_{cc} and d:

$$\begin{cases} V_{C_1} = \dfrac{1-dcc}{(1-2\,dcc)}\,V_{in} \\ V_{C_2} = \dfrac{dcc}{(1-2\,dcc)}\,V_{in} \\ V_{C_3} = V_o = \dfrac{d}{1-2\,d_{cc}}V_{in} \\ I_{L_1} = I_{L_2} = \dfrac{d}{1-2\,dcc}I_o = I_{input} \\ I_{L_3} = I_o \end{cases} \tag{2.5}$$

Then:

$$V_{DC} =< v_{DC} >_T = (1-d_{cc})(V_{C_1} + V_{C_2}) = \frac{1-d_{cc}}{(1-2\,d_{cc})}\,V_{in} \tag{2.6}$$

Since $(1-d_{cc}-d) \geq 0$, it comes that $d \leq (1-d_{cc})$. From (2.5) and (2.6), it is clear that $V_{DC} \geq V_{in}$ and $V_{DC} \geq V_o$. Indeed the input voltage is stepped-up by the QZS stage and subsequently stepped-down by the Buck converter. The inductors of the QZS network (L_1 and L_2) have the same average current. Whenever d_{cc} approaches to 0.5, the ratio V_o/V_{in} does not fulfil anymore (2.5) and (2.6) because of the power losses, then $d_{cc} < \frac{1}{2}$ is required. Once both input and output voltages are fixed, the ratio V_o/V_i is determined, and thanks to (2.6) there is still a degree of freedom for the choice of the values of the two duty cycle values d and d_{cc}, which define the duration of the three operating modes. These two duty cycle values are related each other:

$$d = \frac{V_o}{V_{in}}(1-2\,d_{cc}) \tag{2.7}$$

The optimal relation between the values of d and d_{cc} is found in term of efficiency, by minimizing the power losses and to impose the most convenient command strategy for the proposed QZSBC in the step-up and step-down conversions. The power losses include the losses through the inductors (core and windings, evaluated through the iGSE model [78]), the capacitors and the switches (conduction and switching losses, evaluated as in [79]). However, the power losses model is further detailed in the next chapter.

From (2.7) and the condition $d \leq 1-d_{cc}$, it is possible to obtain the minimum value of the duty cycle d_{cc}:

$$d_{cc} \geq \frac{\dfrac{V_o}{V_{in}} - 1}{\dfrac{2V_o}{V_{in}} - 1} = d_{cc_{min}} \tag{2.8}$$

The value of $d_{cc_{min}}$ is negative for $V_o < V_{in}$, which is impossible. So there are two different ranges of admissible values of d_{cc} depending on the operation mode, boost or buck. In boost operating mode ($V_o > V_{in}$), $d_{cc_{min}}^{(Boost)} = d_{cc_{min}}$ given in (2.8). In buck operating mode ($V_o < V_{in}$), the minimum value of d_{cc} is set to zero ($d_{cc_{min}}^{(Buck)} = 0$).

In order to optimize the duty cycles d and d_{cc} for a given ratio V_o/V_{in}, the QZSBC efficiency maximization is used as criterion. The total power loss $P_{loss}(d_{cc})$ is obtained by summing all the losses contributions, as a function of d_{cc} only; in fact, the duty cycle d is known and can be calculated from (2.7) for a given ratio V_o/V_{in}. For a QZSBC with an output power of 8kW, the Fig. 8 depicts the amount

of the power efficiency as a function of the duty cycle d_{cc} in buck mode ($0 \leq d_{cc} < 0.5$) and boost mode ($d_{cc_{min}}^{(Boost)} \leq d_{cc} < 0.5$) by referring to the system parameters values and components listed in Table 2.1.

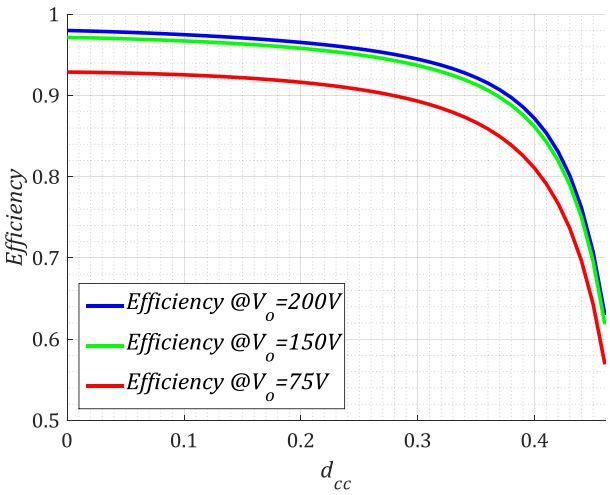
Table 2.1 QZSBC parameters and components employed for the duty cycle values d *and d_{cc} optimization.*

	Operating Point	
V_{in}	Input Voltage	$300V$
V_o	Output Voltage	$[150\,V, 450\,V]$
P_o	Output Power	$8\,kW$
fs	Switching frequency	$30\,kHz$
	Components	
MOSFET switches	CREE - *CAS100H12AM1*	
QZSBC and CUK inductors core	POWERLITE	
	C-Cores	
Capacitors series resistances ESR_{C_i}	$10\,m\Omega$	
Inductors cores	Powerlite C-Cores AMCC-80	
L_1	$403\,\mu H$	
R_{L_1}	$16\,m\Omega$	
$L_2 = M$	$250\,\mu H$	
R_{L_2}	$12.5\,m\Omega$	
L_3	$300\,\mu H$	
R_{L_3}	$7\,m\Omega$	
C_1	$27\,\mu F$	
C_2	$56\,\mu F$	
C_3	$12\,\mu F$	

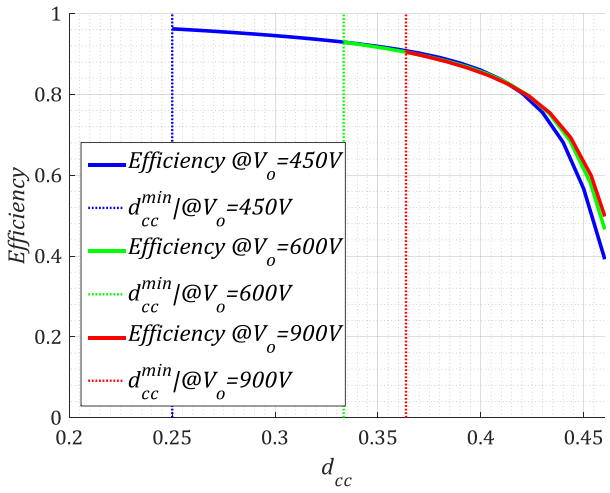
The shorter the duration of the short circuit phase (the duty cycle d_{cc}) is, the smaller are the power losses. Indeed, a greater value of d_{cc} implies higher switching losses of the MOSFET and core losses in L_1 and L_2.

Consequently, for the boost mode operation, the duty cycle d_{cc} is selected equal to $d_{cc} = d_{cc_{min}}^{(Boost)}$ given in (2.8), namely the open circuit mode is suppressed, u_1 is always on, the logic states u_2 and u_k are complementary ($u_1 = 1$ and $u_k = \overline{u_1.u_2} = \overline{u_2}$). So, only the command signal u_2 manages the QZSBC in this mode (Fig. 2.18(a)). In buck mode operation, the d_{cc} is set to zero, short circuit period is deleted, thus the switch *K* is always on ($u_k = 1$) and the switches controlled by u_1 and u_2 operate as a simple buck converter with a second order input filter ($u_2 = \overline{u_1}$). As in the boost mode case, only one signal is enough to control the converter (Fig. 2.18(b)).

A remarkable advantage of this strategy is that the converter can operate with a single signal *u* in both cases, as shown on Fig. 2.18. This implies a great asset in terms of fault-tolerance since the converter can still work in one of the two modes in case of short-circuit of the switch *K* or switch S_1 ($u_K = 1$ or $u_1 = 1$).



(a)



(b)

Fig. 2.17 Power Efficiency in step-down (a) and step-up (b) modes ($V_{in} = 300V, P_o = 8kW, f_s = 30\ kHz$) as a function of d_{cc} ($d_{cc_{min}}^{(Buck)} = 0$ and $d_{cc_{min}}^{(Boost)} = d_{cc_{min}}$ given by (2.8)).

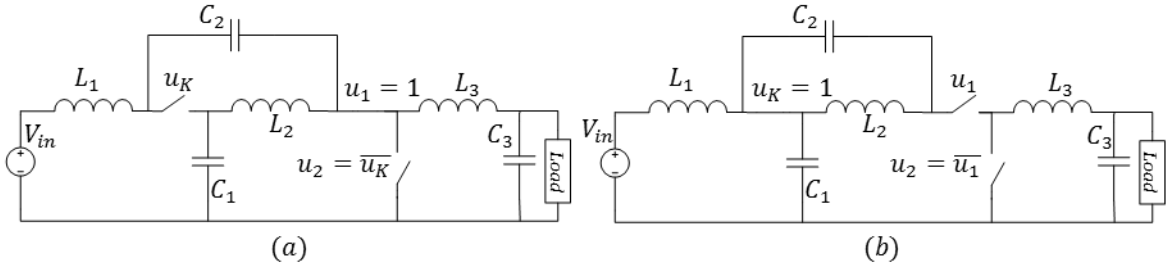


Fig. 2.18 QZSBC command configurations for boost operating mode (a) and buck operating mode (b).

2.3.2 Input ripple suppression

In [70] it is shown that the input current ripple at the switching frequency in a QZS converter can be cancelled with an appropriate magnetic coupling (M) between the inductors L_1 and L_2 ($L_2 = M$). In fact

it can be remarked that the voltage across the two inductors is the same during the whole switching period.

$$v_{L_1}(t) = v_{L_2}(t), \forall t \in [0, T_s] \tag{2.9}$$

In case of a magnetic coupling between the two inductors:

$$v_{L_1} = L_1 \frac{di_1}{dt} + M \frac{di_2}{dt},$$

$$v_{L_2} = M \frac{di_1}{dt} + L_2 \frac{di_2}{dt} \tag{2.10}$$

Then, it is quite straightforward to show that, assuming that the inductors currents are triangular shaped, the input current ripple in L_1 can be suppressed by setting the coupling inductance $M = L_2$:

$$v_{L_1} = L_1 \frac{di_1}{dt} + M \frac{di_2}{dt} \cong L_1 \frac{\Delta i_{L_1}}{\Delta T} + M \frac{\Delta i_{L_2}}{\Delta T},$$

$$v_{L_2} = M \frac{di_1}{dt} + L_2 \frac{di_2}{dt} \cong L_2 \frac{\Delta i_{L_2}}{\Delta T} + M \frac{\Delta i_{L_1}}{\Delta T} \tag{2.11}$$

$$L_1 \frac{\Delta i_{L_1}}{\Delta T} + M \frac{\Delta i_{L_2}}{\Delta T} = L_2 \frac{\Delta i_{L_2}}{\Delta T} + M \frac{\Delta i_{L_1}}{\Delta T} \tag{2.12}$$

$$\Delta i_{L_1} = \frac{L_2 - M}{L_1 - M} \Delta i_{L_2} \tag{2.13}$$

Such a suppression of the input current ripple would allow reducing both cost and volume of the input filter for the high frequency rejection, two key issues for achieving a convenient embedded system.

The design of the C-Cores and the choice of the turn numbers of the coupled inductances have been performed firstly by analytical approach, then the non-saturation condition of the C-cores at the maximal current has been checked by means of 2D Finite Elements Method simulator.

The experimental results performed on a QZSBC prototype in the next section show that this condition is feasible. For the considered case, the ratio between the number of coils in the two windings is such to obtain:

$$L_1 = \frac{3}{2} L_2 \tag{2.14}$$

The same ratio L_1/L_2 is employed for the SEPIC design in Section 2.3.4 for the comparison with the proposed converter topology.

2.3.3 QZSBC experimental validation

Before validating the real prototype, a proper control have been developed and tested in simulation on the system in closed loop. Fig. 2.19 describes the proposed control scheme designed to control the output voltage $v_o = v_{C_3}$.

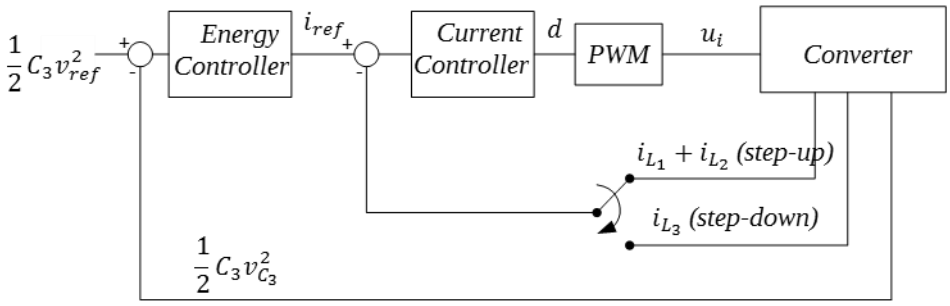


Fig. 2.19 Control scheme implemented for the experimental validation.

This control scheme contains two feedback loops. The control system reference is the electrostatic energy of the capacitor C_3, obtained from the output voltage. The external loop controller (Energy Controller) receives the difference between the electrostatic energy of C_3 and its reference value. It will be shown in the following chapter that it allows a better rejection of the load power disturbances. It provides the current reference to the internal loop, which generates the duty ratio value d. The developed control scheme is suitable for both step-up and step-down configurations. Indeed, the control algorithm switches according to the functioning mode: in step-up mode, the current loop controls the sum of the currents $i_{L_1} + i_{L_2}$, whereas, in step-down mode, it controls the current i_{L_3}. The algorithm switches between step-up and step-down. The smooth transition between the two operating modes (buck and boost) is performed by adding a hysteresis effect to the sign function of the error between the input voltage and the reference voltage. Both controllers are realized by using the indirect Sliding Mode Control [80], [81].

The proposed QZSBC converter has been realized for a DC-DC low power application with variable resistive load and fixed input voltage, where the output voltage can vary in the authorized range mentioned in Table 2.2. The objective of realizing a low power prototype of the QZSBC is to verify its feasibility as well as to perform an efficient control.

Fig. 2.21 shows the steady-state waveforms of inductors currents and capacitors voltages in the QZSBC. As a result of the magnetic coupling between L_1 and L_2, the input current i_{L_1} keeps flat in step-up mode, despite of the current i_{L_2}, which exhibits a ripple at switching frequency.

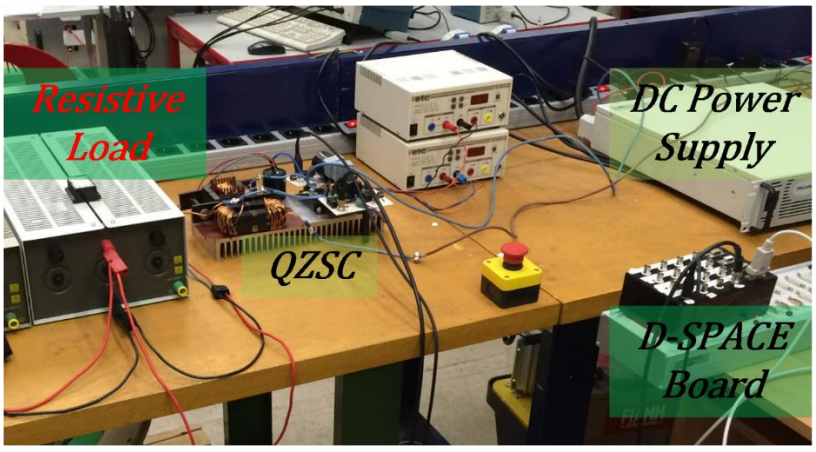


Fig. 2.20 Experimental test bench.

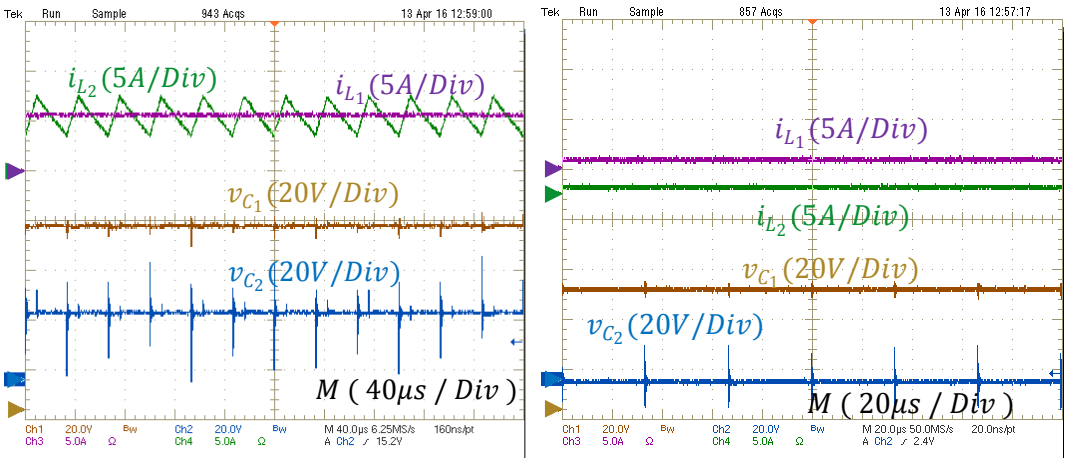
During the step-down mode, both currents i_{L_1} and i_{L_2} stay flats, since the switch S_1 conducts during the whole switching period. The waveforms of v_{C_1} and v_{C_2} are affected by electromagnetic interferences (EMI) due to the switches transient times. Indeed, the active semiconductor switches used for the experimental prototype are SiC based MOSFETs, characterized by extremely fast switching transients.

Table 2.2 Simulation and experimental bench parameters.

Operating Parameters		
$\boldsymbol{V_{in}}$	Input Voltage	$48V$
$\boldsymbol{R_{load}}$	Output Resistance	20Ω
$\boldsymbol{fs}$	Switching frequency	$30\ kHz$
$\boldsymbol{V_o}$	Output Voltage	$[24V\ \div 72\ V]$
$\boldsymbol{\eta}$	Measured Efficiency	$[0.92 \div 0.83]$
$\boldsymbol{P_o}$	Output power	$[30W \div 260\ W]$
Components		
	MOSFET switches	CREE-*CAS100H12AM1*
$\boldsymbol{L_1}$	Coupled Inductance Primary winding	$300\ \mu H$
$\boldsymbol{L_2 = M}$	Coupled Inductance Secondary winding and Mutual inductance	$200\ \mu H$
$\boldsymbol{L_3}$	QZSBC Buck stage inductance	$583\ \mu H$
$\boldsymbol{C_1 = C_2 = C_3}$	QZSBC Capacitors	$680\ \mu F$

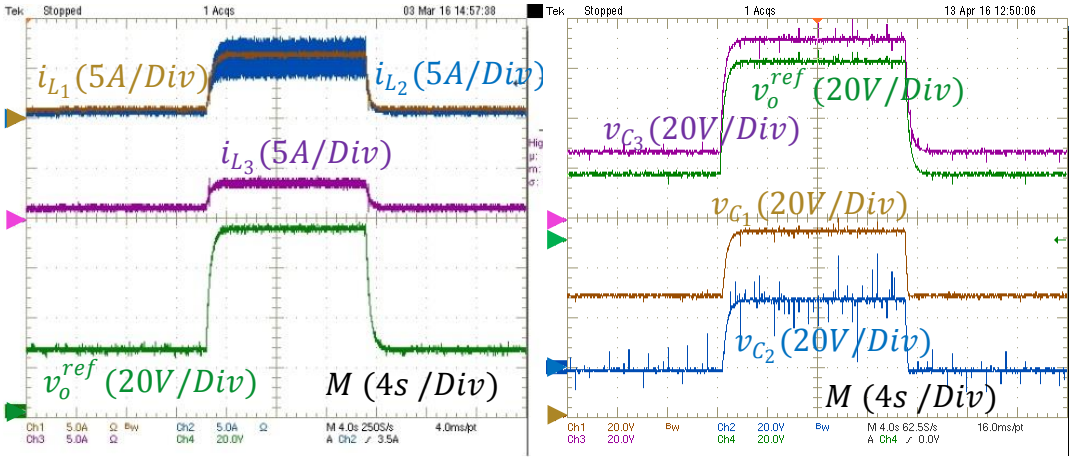
Any EMI filter or additional snubbers have been used in the prototype.

The experimental waveforms of the system variables are shown in Fig. 2.22, when the output voltage reference v_o^{ref} changes from $24\ V$ (buck operation) to $72\ V$ (boost operation) and conversely. The rising and falling time of the reference variation are set to the values required for the considered application ($t_{falling} = t_{rising} = 1\ s$). Fig. Fig. 2.22(b) shows that the output voltage v_{C_3} complies with the reference voltage v_o^{ref}. The other state variables also exhibit a good transition when the algorithm switches between the two equilibrium points.



(a) (b)

Fig. 2.21 Experimental currents and voltages waveforms of $i_{L_1}, i_{L_2}, v_{C_1}, v_{C_2}$ in steady state in boost (a) and buck mode (b).



(a) (b)

Fig. 2.22 Experimental response to the output voltage reference variation of the currents (a) and of the voltages (b).

2.3.4 Comparison

The comparison between the converters concerns the electrical stresses through the passive and active components, expressed as function of the voltage gain:

$$\alpha = \frac{V_o}{V_{in}} \tag{2.15}$$

The operating point values which describe the application previously discussed are reported in Table 2.3. The power load is a simple resistor, which broadly corresponds to the requirement of load power described in Fig. 2.7 as function of the output voltage.

Table 2.3 Operating point of the two converters for the stored energy and efficiency comparison..

Operating Point		
$\boldsymbol{V_{in}}$	Input Voltage	$300V$
$\boldsymbol{V_o}$	Output Voltage	$[150\,V, 450V]$
$\boldsymbol{R}$	Output resistive load	10Ω
$\boldsymbol{f_s}$	Switching frequency	$30\,kHz$

The following ripple specifications are accounted for the conducted analysis:

- $\Delta v_C \leq 3\%\, V_C$ for the capacitors voltage ripple, with V_C as the capacitor DC voltage value;
- $\Delta i_i = \Delta i_{L_1} = 0$ for the input current ripple, (L_1 in the three converters);
- $\Delta i_L \leq 40\%\, I_L$ for all inductances but the input ones, where I_L is the inductance DC current value at the maximal power (at $v_o = V_{o_{max}}$).

The inductors' voltage seconds integrals λ_{L_i} and the charge absorbed ΔQ_{C_i} by each capacitor are useful quantities to compare the current and voltage ripples on the passive components of the converters under analysis:

$$\lambda_{L_i}^{(charge)/(discharge)} = \int v_{L_i}\, dt, \qquad \Delta Q_{C_i}^{(charge)/(discharge)} = \int i_{C_i}\, dt \tag{2.16}$$

These values impact on the inductances and capacitances values, then on the stored magnetic and electrostatic energy, along with the DC current and voltages. It is clear that in steady state the integrals evaluated in a whole switching period are equal to zero, then:

$$\lambda_L^{(charge)} + \lambda_L^{(discharge)} = 0, \qquad \Delta Q_{C_o}^{(charge)} + \Delta Q_{C_o}^{(discharge)} = 0 \tag{2.17}$$

Then:

$$\Delta i_{L_i} = \frac{\left|\lambda_{L_i}^{(charge)}\right|}{L_i} = \frac{\left|\lambda_{L_i}^{(discharge)}\right|}{L_i}, \qquad \Delta v_{C_i} = \frac{|\Delta Q_{C_i}^{(charge)}|}{C_i} = \frac{|\Delta Q_{C_i}^{(discharge)}|}{C_i} \tag{2.18}$$

From (2.18) it can be deducted that the greater the λ_{L_i} and ΔQ_{C_i} values, the greater the L_i and C_i values to ensure low ripple values Δi_{L_i} and Δv_{C_i}.

The following Table, besides the mentioned values λ_{L_i} and ΔQ_{C_i}, describes the voltage and current stresses across the active and passive components as function of the voltage gain α. The D values relative to the QZSBC topology represent the complementary values of the duty cycle of S_2, then the duty cycle of S_1 in step-down mode and of S_k in step-up mode.

The passive components shall be designed for the worst operating case in the output voltage range, hence voltage gain α range, specified in Table 2.3. In order to comply with the ripple requirements specified above, the capacitance and inductance values have been chosen as in Table 2.5. The evaluated performances of CUK and SEPIC, in terms of efficiency and stored energy, are very similar. For this reason, it was considered sufficient to treat and compare only the performances of the SEPIC converter.

As showed in Fig. 2.23, the inductors currents and capacitors voltages ripples are evaluated as in (2.18) as function of the voltage gain α. The obtained evaluations show that the aforementioned requirements are satisfied for the whole range of the voltage gain. The simulation results in Fig. 2.24 and Fig. 2.25 confirm the compliance with the ripple constraints at $V_o = 150V$ and $V_o = 450V$ for both converters. The ripple condition is not respected only for the QZSBC capacitor C_2 in buck mode, since its DC voltage is $V_{C_2}^{(step-down)} = 0$.

Two main aspects shall be now considered, namely efficiency and stored energy. As further discussed in the next chapter, the size of a passive component grows monotonously with its energy rating. In Fig. 2.26, the sum of the electrostatic and magnetic energies of the passive components is evaluated for the whole range of voltage V_o in steady state for the two converters. It is worth mentioning that, for a coupled inductor, the stored energy is defined as:

$$E_L = \frac{1}{2} L_1 i_{L_1(\max)}^2 + \frac{1}{2} L_2 i_{L_2(\max)}^2 + M\, i_{L_1(\max)}\, i_{L_2(\max)} \tag{2.19}$$

The energy stored clearly reaches its maximum at $V_o = 450V$. The results reveal that, for the considered application, in both step-up and step-down operations, the magnetic and electric energies, stored in the passive components of the QZSBC, are lower than the ones stored in passive components of the SEPIC converter. In the SEPIC converter, most of the contribution of stored energy is provided by the output capacitor C_2, because of its great value. Indeed, it shall be designed to filter the discontinuous current conducted by the diode and respect the constraint on the output voltage ripple. Even with a higher number of inductors, the magnetic energy stored by the QZSBC is lower in the considered range of α, mostly because of the smaller values of inductances required to respect the

constraint on the inductors' current ripples. Anyway, this application was conceived for a low voltage gain. In applications where a higher output voltage is required, the considerations concerning the magnetic energy are not true anymore, and either a SEPIC or CUK topology could be preferable.

Table 2.4 Comparative analysis between QZSBC, SEPIC and CUK.

	QZSBC		*CUK*	*SEPIC*
	Buck Mode	***Boost Mode***		
Duty cycle	$D^{(S_1)} = \alpha$	$D^{(S_k)} = \frac{\alpha}{2\alpha - 1}$	$D^{(S_1)} = \frac{\alpha}{\alpha - 1}$	$D^{(S_1)} = \frac{\alpha}{\alpha - 1}$
Inductors average currents	$I_{L_1} = I_{L_2} = \frac{P_o}{V_{in}}$ $I_{L_3} = \frac{P_o}{\alpha\, V_{in}}$	$I_{L_1} = I_{L_2} = \frac{P_o}{V_{in}}$ $I_{L_3} = \frac{P_o}{\alpha\, V_{in}}$	$I_{L_1} = \frac{P_o}{V_{in}}$ $I_{L_2} = \frac{P_o}{\alpha\, V_{in}}$	$I_{L_1} = \frac{P_o}{V_{in}}$ $I_{L_2} = \frac{P_o}{\alpha\, V_{in}}$
λ_{L_i} (CCM)	$\lambda_{L_1} = \lambda_{L_2} = 0$ $\lambda_{L_3} = \frac{V_{in}\,\alpha\,(\alpha - 1)}{f_s}$	$\lambda_{L_1} = \lambda_{L_2} = \lambda_{L_3}$ $= \frac{V_{in}}{f_s}\frac{\alpha(\alpha - 1)}{(2\alpha - 1)}$	$\lambda_{L_1} = \lambda_{L_2}$ $= \frac{V_{in}}{f_s}\frac{\alpha}{(\alpha - 1)}$	$\lambda_{L_1} = \lambda_{L_2}$ $= \frac{V_{in}}{f_s}\frac{\alpha}{(\alpha - 1)}$
Capacitors average voltages	$V_{C_1} = V_{in}$ $V_{C_2} = 0$ $V_{C_3} = \alpha V_{in}$	$V_{C_1} = \alpha V_{in}$ $V_{C_2} = V_{in}(\alpha - 1)$ $V_{C_3} = \alpha V_{in}$	$V_{C_1} = V_{in}(\alpha + 1)$ $V_{C_2} = \alpha V_{in}$	$V_{C_1} = V_{in}$ $V_{C_2} = \alpha V_{in}$
ΔQ_{C_i} (CCM)	$\Delta Q_{C_1} = \frac{I_{L_1}(1 - D)}{f_s}$ $\Delta Q_{C_2} = \frac{I_{L_2}(1 - D)}{f_s}$ $\Delta Q_{C_3} = \frac{\Delta i_{L_3}}{8\, f_s}$	$\Delta Q_{C_1} = \frac{I_{L_2}(1 - D)}{f_s}$ $\Delta Q_{C_2} = \frac{I_{L_1}(1 - D)}{f_s}$ $\Delta Q_{C_3} = \frac{\Delta i_{L_3}}{8\, f_s}$	$\Delta Q_{C_1} = \frac{I_{L_1} D}{f_s}$ $\Delta Q_{C_2} = \frac{\Delta i_{L_2}}{8\, f_s}$	$\Delta Q_{C_1} = \frac{I_{L_1} D}{f_s}$ $\Delta Q_{C_2} = \frac{I_{L_2} D}{f_s}$
Hard switched devices' reverse-voltage stress	$V_{S_1} = V_{in}$	$V_{S_k} = V_{in}(\alpha + 1)$	$V_{S_1} = V_{in}(\alpha + 1)$	$V_{S_1} = V_{in}(\alpha + 1)$
Hard switched devices' maximal conduction current	$i_{S_1}^{(max)} = I_{L_3} + \frac{\Delta i_{L_3}}{2}$	$i_{S_k}^{(max)}$ $= I_{L_1} + I_{L_2} + \frac{\Delta i_{L_2}}{2}$	$i_{S_1}^{(max)}$ $= I_{L_1} + I_{L_2} + \frac{\Delta i_{L_2}}{2}$	$i_{S_1}^{(max)}$ $= I_{L_1} + I_{L_2} + \frac{\Delta i_{L_2}}{2}$

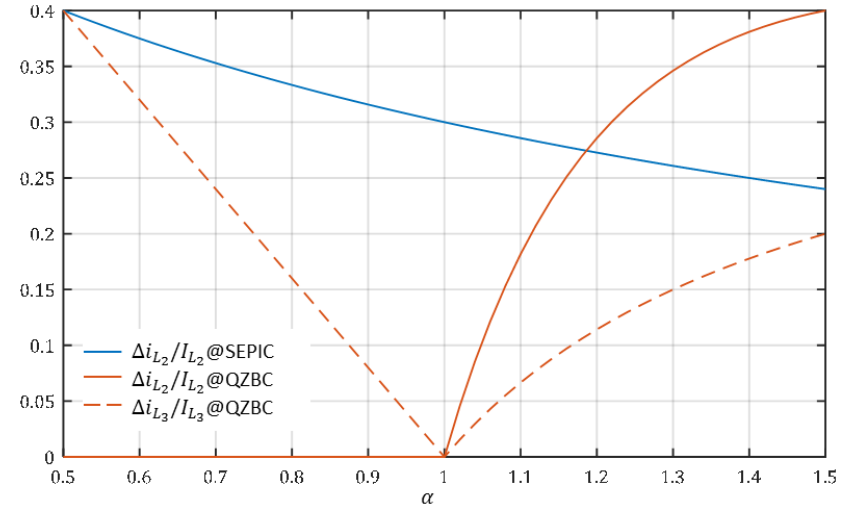
Table 2.5 Passive components values for the compliance with the specified ripple constraints.

	QZSBC	*SEPIC*
L_1	526 μH	1.2 mH
$L_2 = M$	351 μH	2.1 mH
L_3	1.1 mH	-
C_1	16 μF	40 μF
C_2	49 μF	26 μF
C_3	2.2 μF	-

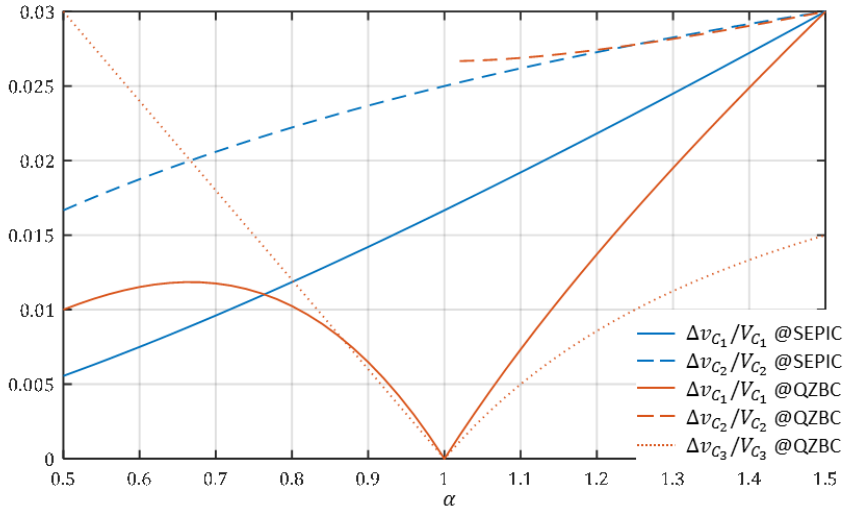
The power losses depend on numerous design choices, such as the switching frequency, the magnetic cores and the relative parameters, and so on. Anyway, in the case of non-isolated SMPS, the most part of the power losses is mostly attributable to the switching devices. It is then worth to analyse and compare the current and voltage stresses on the power devices. Namely, it shall be considered the RMS currents for the conduction losses and the voltage and current stresses across the hard switched device (for the QZSBC the hard switched device is S_1 in step-down mode and S_k in step-up, S_1 for the SEPIC).

The QZSBC has three active switches, nevertheless only two are alternatively switched. In buck mode, the S_1 and S_2 RMS currents in the QZSBC showed in Fig. 2.27 are lower than the CUK and SEPIC ones in the whole range of voltage, which suggest lower conduction losses.

During the step-down operating mode, as shown in Table 2.4, the reverse voltage and the maximal conduction current across the QZSBC hard switched device in off-state is lower as well, hence the switching losses in the QZSBC device result lower than the SEPIC hard switched transistor S_1. In boost mode, the voltage across the hard switched device is the same in the two converters, but the maximal current is higher for the QZSBC converter S_k device. Then, in boost mode, the efficiency of the two converters at the maximum voltage gain α would depend on the selected devices. Nevertheless it should be remarked that the QZSBC has been proposed for the mission profile reported in Fig. 2.7, then the step-up operation occurs in a small fraction of the cycle period. The efficiency shall be measured on the whole cycle, where the step-down operation is mostly required, for which the proposed QZSBC topology is clearly advantageous.

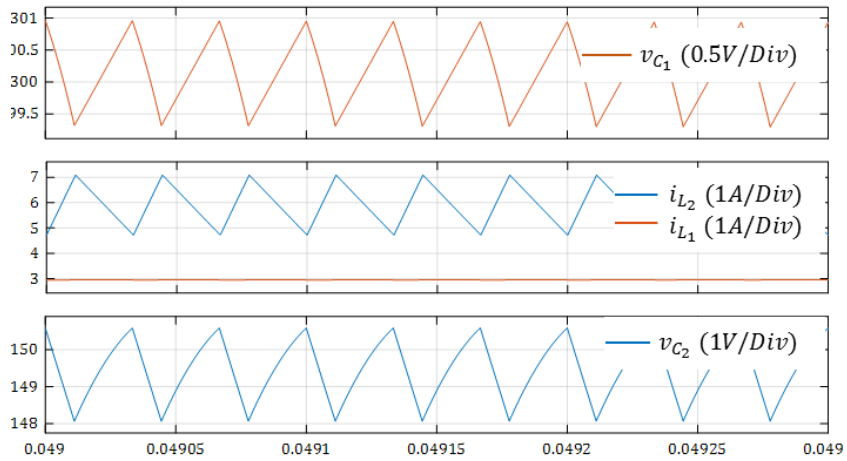


(*a*)

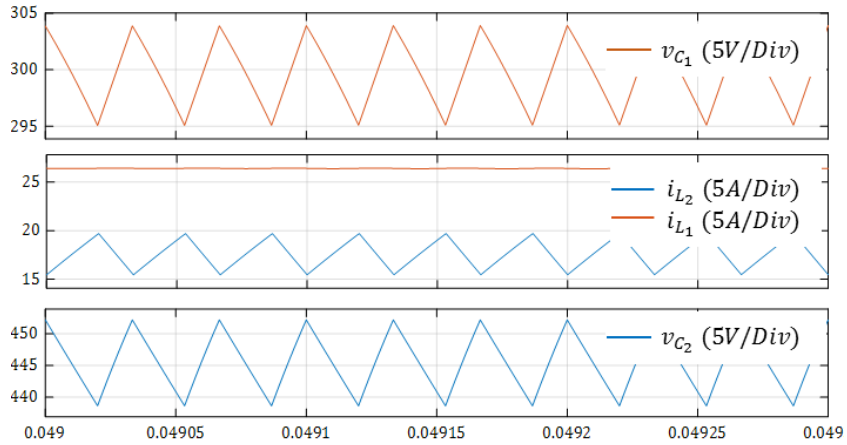


(*b*)

Fig. 2.23 Current ripple rate $\Delta i_{L_i}/I_{L_i}$ (a) and voltage ripple rate $\Delta v_{C_i}/V_{C_i}$ (b) as function of the voltage gain range.



(a)



(b)

Fig. 2.24 QZSBC (a) and SEPIC (b) waveforms with the capacitance and inductance values specified in Table 2.5 and the operating point in Table 2.3 ($V_o = 150V$).

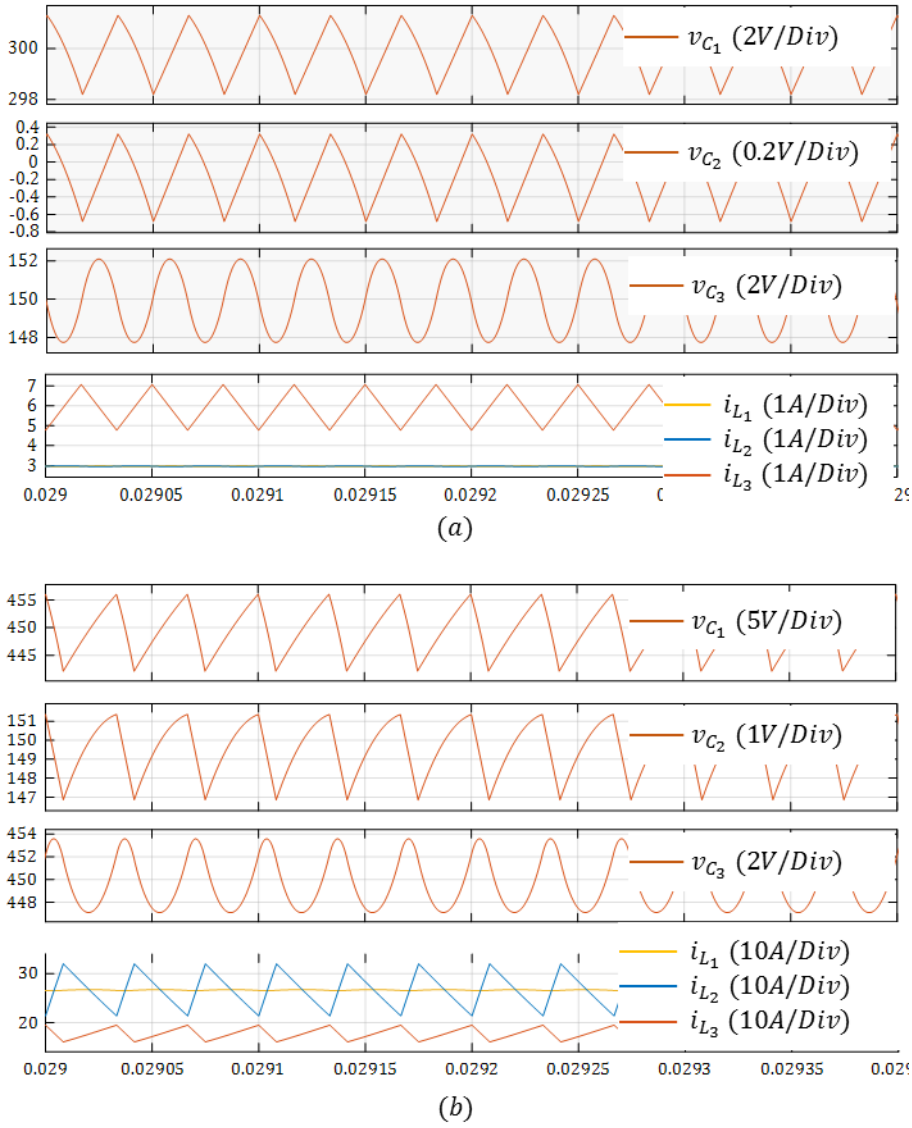


Fig. 2.25 QZSBC (a) and SEPIC (b) waveforms with the capacitance and inductance values specified in Table 2.5 and the operating point in Table 2.3 ($V_o = 450V$).

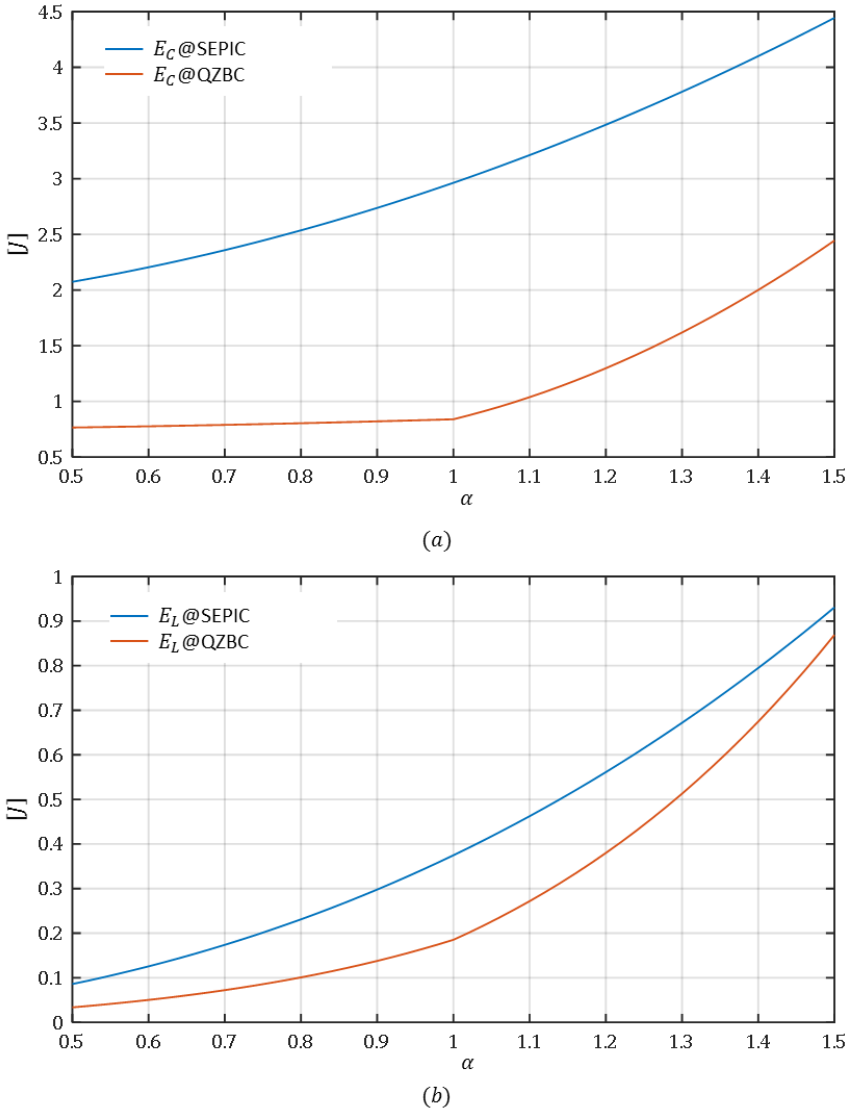


Fig. 2.26 Static energy (a) and magnetic energy (b) amount stored in the two converters, as function of the voltage gain.

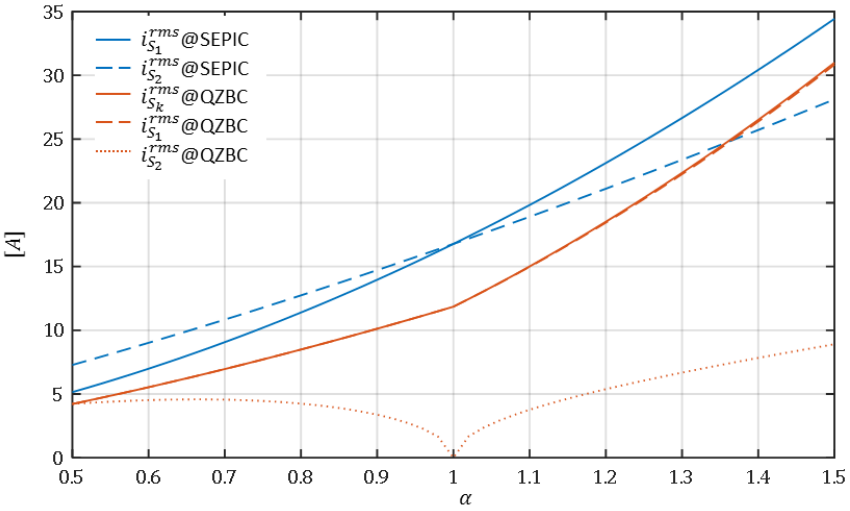


Fig. 2.27 Devices RMS currents comparison as function of the voltage gain.

2.4 Conclusions

In this chapter, the role of the DC/DC conversion in a motor supply frame has been discussed. In a powertrain actuator for embedded applications as MEA or EV/HEV, the possibility to control the DC voltage upstream the DC/AC inverter provide several advantages, such as the reduction of the power losses and the size of the power conversion chain. Furthermore, a PAM for the command signals generation has the opportunity to be implemented, which allows to reduce the number of commutations of the inverter devices within the mechanical period of the AC load, in this case a PMSM, and decreases the distortion of the current ripple in the motor windings, which is deleterious for the motor itself and for the torque control. The most classical DC/DC converter architectures have been presented for the considered task. Depending on the mission profile, it could be more advantageous a step-up converter for a high speed application, or a step-up/down for a wide speed range application.

A new topology of step-up/down converter based on the joint use of a Quasi Z-source converter and a DC/DC Buck converter for a motor driving application has been presented and analysed. The proposed QZSBC is an interesting topology when the step-up/down feature is required for a mainly step-down mode. Indeed, the operating cycle application requires a low motor speed for the main part of the cycle, hence the DC/DC stage has to provide mainly a low output voltage. For a brief portion of the whole cycle period, the converter supplies a high output voltage in order to allow the actuator reaching higher speeds. Furthermore, the coupled inductors version of the topology allows to suppress the input current ripple at the switching frequency, which provides a great gain of mass on the design of the EMI input filter. A converter prototype has been realized and the experimental results show its feasibility.

The QZSBC converter has been compared with a classical non-inverting step up-down SEPIC converter. This topology has been chosen because of the common feature concerning the continuous input current and the possibility to suppress the input current ripple. The comparison has been led in order to show the voltage and current stresses across the converters active and passive components for a given range of voltage gain. The amount of magnetic and electrostatic energy stored by the passive components show that the QZSBC stores less energy which means that, due to the relation between stored energy and size of the passive components (detailed in the next chapter), the QZSBC requires smaller capacitors and inductors for the considered operating range. Furthermore, the analysis of the RMS currents and reverse voltages on the hard-switched devices suggests that the power losses in the proposed converter are lower for the step-down operating range and comparable for the step-up mode. Then, the efficiency of the QZSBC measured on an entire mission cycle will result higher than the SEPIC one, which means that the converter has globally better performances in the mentioned application.

3 DC/DC Power Converter Design

3.1 Introduction

In this chapter the design approach of a DC/DC converter is discussed for the application described in the previous chapter, namely for a powertrain conversion chain for a starter motor. Anyway, the insertion of an extra converter does not come without inconveniences. The DC/DC converter should be indeed opportunely designed and optimized as well. A consistent part of the chapter is indeed reserved to the description of the design of the DC/DC converter power stage, specifically a Boost converter. The main subject of the thesis work deals with the optimization of efficiency and size of the DC/DC conversion unit. The method to select converter active and passive components and the analytical models adopted for the evaluation of the power losses should be thoroughly presented, in order to provide a global vision of the multiple design parameters and choices at stake and the interdependencies between them. Indeed, the design of each DC/DC converter is a non-trivial problem. A global knowledge of the design choices and parameters involved in the selection of each element of the converter and their impact on the converter performances are required to attain a reliable and optimal design. The continual development of power electronic converters is driven by the requirements for higher efficiency, lower volume, lower weight and lower production costs. A high efficiency is usually demanded at the nominal operating point to ensure a wise use of the energy resources and a low operating cost. To reach such objectives it is mandatory to lighten the bulky part of the power electronics, namely the passive elements and the heat sink, and simultaneously reduce the lost energy as much as possible. The efficiency aspects refer to the active component losses, reduction of both conduction and switching losses are expected with a view to downsize the heatsink. In the field of electric or hybrid vehicles, aerospace and any kind of on-board power supplying applications, the autonomy is of prime importance. In this type of applications, it is paramount to implement power electronics converters with the highest efficiency. Moreover, embedded systems should be equipped with power electronics converters as lighter and smaller as possible. This feature refers to a high compactness and power density characteristic of the converter. These efficiency and compactness criteria stand for the framework and the context of the proposed thesis. A power electronic converter is formed from the following main elements:

- Power Semiconductor Modules
- Modulation and Control Circuit / Auxiliaries
- Power passive components (Filter Components, Transformers)
- Cooling System
- Interconnection / Packaging

Power electronics converters are strongly heterogeneous systems (power semiconductors, electrical and magnetic energy storages, etc.) and hence depend on numerous technologies. Several technological steps lead development trends in power electronics converters. The research effort, indeed, focused on several fields, and each innovative contribution led to new improvements of the power conversion systems. Some examples of significant innovations in the last decade are:

- New magnetic materials: Amorphous and nanocrystalline materials offered the opportunity for the creation of magnetic cores more efficient and more performant in a wide range of frequencies [82].
- Wide bandgap devices: the recent advances in wide bandgap technology created the best opportunities for increasing the converters performances; WBG devices, such as silicon carbide (SiC), have properties that are superior to those of Si, as explained in Chapter 1.

- Integration level improvement: Converters' compactness is remarkably improved by integrating multi-functional elements, such as integrated EMC filters, planar inductors and transformers, integrated heatsink (cold plate), or by developing new integrated packaging parts that perform packaging functions (electrical interconnection, insulation, mechanical support, and protection) for more elements and with extra-functions (lead frames, heat removal etc.) [83].

In the same direction, consistent efforts moved toward the improvement of the designers' tools and analysis methods. The increase of the calculators' power and performances offered several instruments to predict the magnetic, electrical and thermal behaviour of the elements, Finite Element Method (FEM) and computational Fluid Dynamics etc. [84]–[88], which are used to solve governing equations for electric, thermal, electromagnetic, and mechanical problems. These tools and the technological improvements help to improve the performances of the fundamental elements of the converter.

Yet, the design of a power converter remains a challenging task. Even for a simple architecture, the involvement of several design choice in such a heterogeneous field, leads to consider a large number of parameters, relative to each component and part of the system. The understanding of all the phenomena and the intermingled effects of these parameters depend only on the experience and the knowledge of the designer. Therefore, this section aims to address the considerations to be taken into account during the design phase of a simple DC-DC converter, namely a boost converter. The design of a single component cannot be analysed individually or isolated from the rest of the design. Rather, it should be underlined the consequences that certain choices will have on the sizing of the remaining parts of the converter.

Besides the several parameters involved in the design of each element, the following sections present the performance models employed in this thesis work. Since the motivation of this work is efficiency and compactness, the proposed method for the evaluation of the power losses of each component is described, as well as the influence of the design parameters on the size of the passive elements and the cooling unit.

3.2 DC-DC Boost Converter Design

The following section deals with the design of a classic DC-DC bidirectional boost converter, as shown in Fig. 3.1. It is a magnetic storage switched-mode power supply, whose operation principle is briefly reminded hereafter. The steady state currents through the inductor L and the switches S_1 and S_2 are showed in Fig. 3.2.

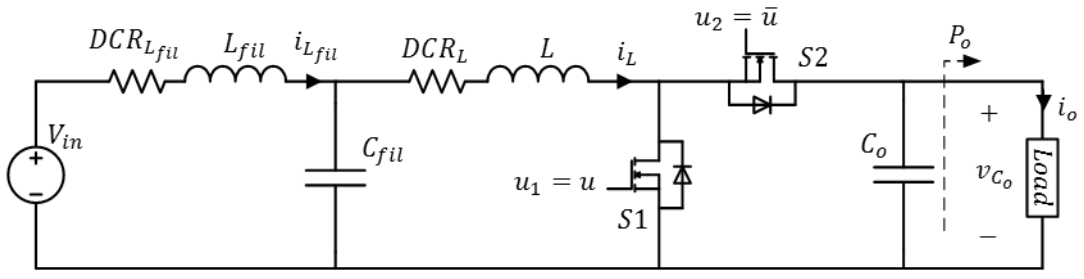


Fig. 3.1 Boost Converter and LC input filter.

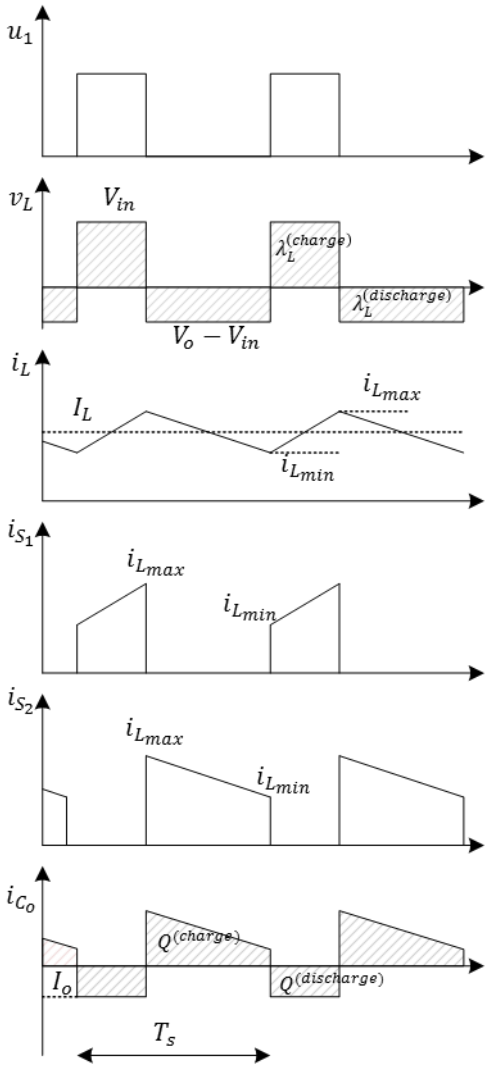


Fig. 3.2 Steady state current waveforms in a DC/DC Boost converter.

The power stage of the system is composed by the converter (an inductor L, a capacitor and two semiconductor-based components), the LC input filter and the load. The power load consists of the assembly DC/AC converter (VSI) and PMSM, whose current response (torque response) is supposed to be very fast, then it can be modelled by a constant power load for any operating point. However, since this chapter deals with only the steady state behaviour, the power load dynamic does not affect the following analysis. The alternate conduction of the switches within the switching period T_s determines the storage and the release of the magnetic energy in the inductor L. The energy gathered during the conduction of the switch S_1 is released during the conduction of the switch S_2.

The design has to be conducted in order to fit with the operating point constraints, as well as the constraints relative to the current and voltage waveforms at the input and the output terminals (ripple values). The operating point requirements considered in this chapter include fixed input and output voltages and the ripple requirements on the output voltage and the input current, as specified in Table 3.1. In the following notations, the average values of the converter currents and voltages are addressed in uppercase (ex. $< i_L >_{T_s} = I_L, < i_o >_{T_s} = I_o, < v_{C_o} >_{T_s} = V_o$ etc.).

Usually, the traditional DC/DC converter design approach consists in the identification of suitable electronic components assuring a correct behaviour and the compliance with the required performances. In this section the main parts of the considered system are described to understand all the variables and all the interdependencies involved in order to provide a better understanding of the necessary trade-offs in the design.

Table 3.1 Operating parameters of the converter.

Symbol	Description
V_{in}	Input voltage
V_o	Average Output voltage
P_o	Average Load power
I_o	Average Load current
$I_{in} =< i_L >_{T_s} =< i_{L_{fil}} >_{T_s}$	Input current
$D = 1 - \frac{V_{in}}{V_o}$	Duty cycle, ($D' = 1 - D$)
$\Delta i_L = \frac{D\, V_{in}}{f_s\, L}$	Current ripple of the L inductor
$\Delta v_{o_{lim}}$	Output voltage ripple limit
$\Delta i_{i_{lim}}$	Input current ripple limit

3.3 Active components

In a switched mode energy converter, the configuration of the architecture is periodically mutated within the switching period T_s through the use of switching devices. This allow the exchange of energy between the passive components of the converter. One of the targets of this thesis study is to show the impact of using the SiC MOSFETs in the design of a power converter for embedded applications. As mentioned in the first chapter, the SiC MOSFET unipolar device is characterized by a very fast switching behaviour and a low conduction voltage. These features lead to low switching and conduction power losses, compared to the Si IGBT devices (for the same current and voltage ratings). For this reason, the only MOSFETs devices are considered and analysed. In this section, the power losses model employed will be discussed, with a particular emphasis on the switching behaviour. Like all power semiconductor elements, the transistor MOSFET exhibits parasitic elements that cannot be overlooked. As already mentioned, these elements include intrinsic capacitances C_{GS}, C_{GD} and C_{DS} whose charging and discharging processes govern the switching behaviour and the switching energy losses of the device. In conduction state, the MOSFET is considered as a resistive path with resistance r_{DS}, usually defined in the device datasheet.

3.3.1 MOSFET conduction behaviour

In a switched-mode power supply (SMPS), during the normal conduction, the MOSFET works with a low voltage drop across the drain-source terminals, hence in the triode region of the typical output characteristic. Within this region, its behaviour is linear and it is practically equivalent to a resistance r_{DS}, provided by the manufacturer. The conduction power losses of the generic S_i device are defined as:

$$P_{S_i}^{(conduction)} = r_{DS}\, i_{DS}^{rms2} \tag{3.1}$$

Where i_{DS}^{rms} is the rms current through the device.

The conduction power losses evaluated for the two transistors S_1 and S_2 are:

$$P_{S_1}^{(conduction)} = r_{DS}\, D \left(I_L^2 + \frac{\Delta i_L^2}{12} \right) \tag{3.2}$$

$$P_{S_2}^{(conduction)} = r_{DS}\, D' \left(I_L^2 + \frac{\Delta i_L^2}{12} \right) \tag{3.3}$$

3.3.2 MOSFET switching behaviour

The MOSFET behaviour during the switching transients is strongly influenced by the intrinsic capacitances of the device.

The following analysis is carried out under the condition of an inductive current, since it is the most common case in practice. The driver circuit is assumed to deliver constant voltages, providing V_{dr} in turn-on and 0 in turn-off, and r_g is the gate-resistance composed by the series connection of the internal gate resistance (provided by the constructor datasheet) and the external driver resistance.

In a bi-directional boost converter, the low MOSFET S_1 commutates in hard-switching, hence the drain-source voltage v_{DS} abruptly changes between the conduction voltage drop to/from the nominal reverse voltage $v_{DS_{S_1}}^{(off)} = V_o$.

Thanks to the conduction of the high diode during the dead band time, the high MOSFET S_2 transition occurs instead in soft switch, i.e. the reverse voltage during the commutation amounts to the only diode bias voltage $v_{DS_{S_2}}^{(off)} = -V_D$. The switching energy loss in S_2 results indeed widely lower than the S_1 one.

Consequently, only the switching behaviour of S_1 is discussed.

3.3.2.1 Turn-on

After the command signal to the gate terminal increases to V_{dr}, $v_{GS_{S_1}}$ starts rising. Once the v_{GS} rises beyond the threshold voltage, the current in the MOSFET channel starts increasing, until it reaches the value $i_{L_{min}}$. During this interval, the voltage $v_{DS_{S_1}}$ is clamped at V_o by the freewheeling diode D_2. Once the current in the diode D_2 becomes zero and the diode is blocked, the MOSFET voltage starts decreasing, and the $C_{GD_{S_1}}$ start discharging. In this lapse of time (*miller plateau*) the gate current flows just through the $C_{GD_{S_1}}$ capacitor, hence the gate voltage $v_{GS_{S_1}}$ does not change until the end of the $v_{DS_{S_1}}$ fall. An indicative evolution of the S_1 MOSFET voltage and current waveforms is shown in Fig. 3.3.

During the period $t_{on_{S_1}}$, the current i_g through the resistance R_g applied to the gate is considered to have a constant value:

$$i_g^{(on)} = \frac{V_{dr} - v_{sp_{S_1}}^{(on)}}{R_g} \tag{3.4}$$

Where $v_{sp_{S_1}}^{(on)}$ is the gate-source voltage value during the *miller plateau*. $v_{sp_{S_1}}^{(on)}$ is assumed to have a constant value and in literature it is often evaluated as follow [79], [89], [90]:

$$v_{sp_{S_1}}^{(on)} = V_{th} + \frac{i_{DS_{S_1}}}{g_{f_s}} \tag{3.5}$$

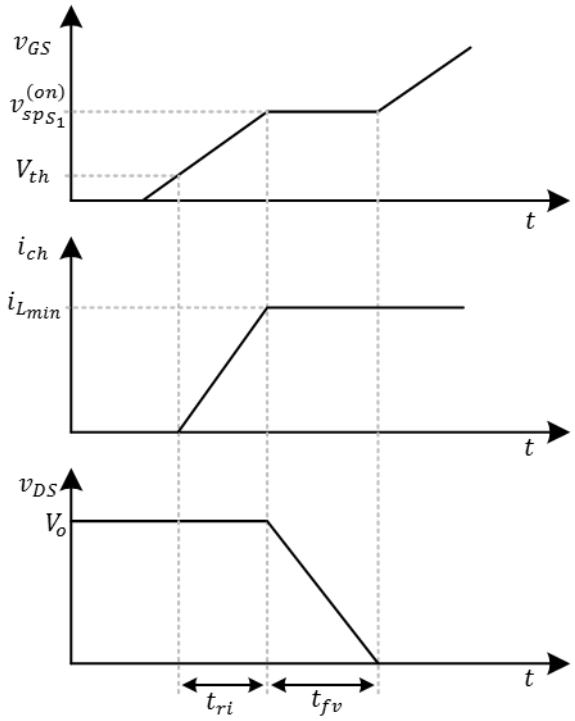


Fig. 3.3 MOSFET turn on waveforms.

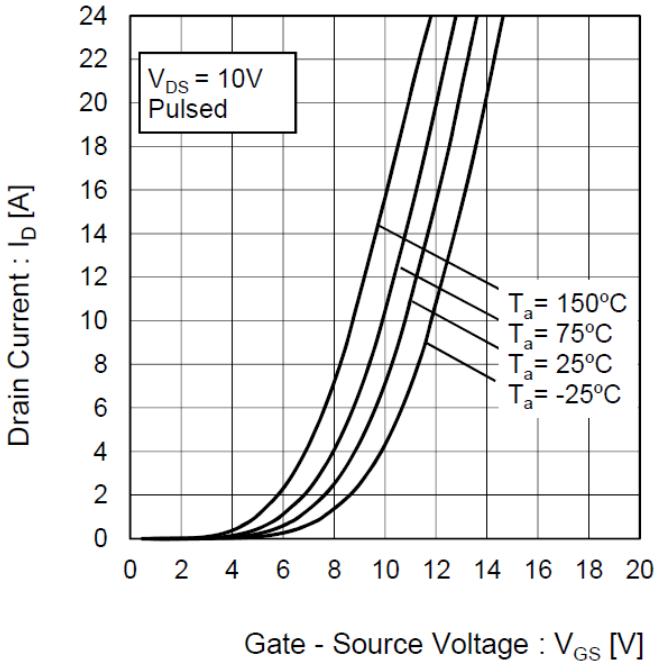


Fig. 3.4 MOSFET trans-conductance characteristic (i_{DS}/v_{GS}) of a ROHM SiC power MOSFET SCT2120AF [91].

Where g_{f_s} is the channel trans-conductance, V_{th} is the gate threshold voltage over which the channel starts conducting and $i_{DS_{S_1}} = i_{L_{min}}$ is the current through the MOSFET channel when fully switched on.

The trans-conductance value g_{f_s} is visibly related to the operating point, namely to the drain-source current value $i_{DS_{S_1}}$, as shown in the characteristic provided by a manufacturer (Fig. 3.4). Then g_{f_s} can be expressed as function of $i_{DS_{S_1}}$:

$$g_{f_s} = \frac{\partial i_{DS_{S_1}}}{\partial v_{GS_{S_1}}} = g_{f_s}(i_{DS_{S_1}}) \tag{3.6}$$

The alternative approach adopted in the following analysis, similarly treated in [92], aims to obtain a way to evaluate the *plateau* voltage v_{sp} as explicit function of i_{DS}. The common expression of the i_{DS} current (in a general case) in saturation state of the MOSFET ($v_{DS} > v_{GS} - V_{th}$) is given in (3.7), where the pinch-off effect on the MOSFET channel has been neglected (it would lead to a more complex equation [79]):

$$i_{DS}|_{@(saturation)} = \kappa_{ch}(v_{GS} - V_{th})^2 \tag{3.7}$$

The constant κ_{ch} is function of the electron mobility (for a n MOSFET), the oxide capacity per unit area and the geometrical factor of the MOSFET [79]. This value can be easily extracted from an arbitrary point of the manufacturer datasheet trans-conductance characteristic, as the one shown in Fig. 3.4. From (3.7):

$$v_{GS} = V_{th} + \sqrt{\frac{i_{DS}}{\kappa_{ch}}} \tag{3.8}$$

The *miller plateau* voltage is given by:

$$v_{sp_{S_1}}^{(on)} = V_{th} + \sqrt{\frac{i_{L_{min}}}{\kappa_{ch}}} \tag{3.9}$$

Such expression of the *Miller plateau* $v_{sp_{S_1}}^{(on)}$ is valid for a wider operating current range than the expression (3.5). When it comes to deal with several design solutions, for example different values of current ripples, hence switching current i_{DS}, the proposed method is more immediate and practical. Moreover, it does not involve the inaccuracies due to the local approximation of the g_{fs} trans-conductance value.

The switching time $t_{on_{S_1}} = t_{ri} + t_{fv}$ is deducted dividing the amount of charge accumulated during this period in the capacitance $C_{iss} = C_{GS} + C_{GD}$ by the current $i_g^{(on)}$ supplied by the driver:

$$t_{ri} = \frac{Q_{GS}}{i_g^{(on)}}, \qquad t_{fv} = \frac{Q_{GD}}{i_g^{(on)}}, \qquad t_{on_{S_1}} = \frac{Q_{GS} + Q_{GD}}{i_g^{(on)}} \tag{3.10}$$

The value of electric gate charge Q_{GS} and Q_{GD} absorbed by the gate as function of the v_{GS} voltage is available in the device datasheet, as in Fig. 3.5.

The power losses $P_{on}^{(S_1)}$ referred to the turn-on transition are evaluated as:

$$P_{on}^{(S_1)} = \frac{1}{2} i_{L_{min}} V_o \, t_{on_{S_1}} f_s \tag{3.11}$$

For the soft switched S_2 MOSFET:

$$P_{on}^{(S_2)} = \frac{1}{2} i_{L_{max}} V_D \, t_{on_{S_2}} \, f_s \tag{3.12}$$

Where $t_{on_{S_2}}$ is evaluated through the same procedure.

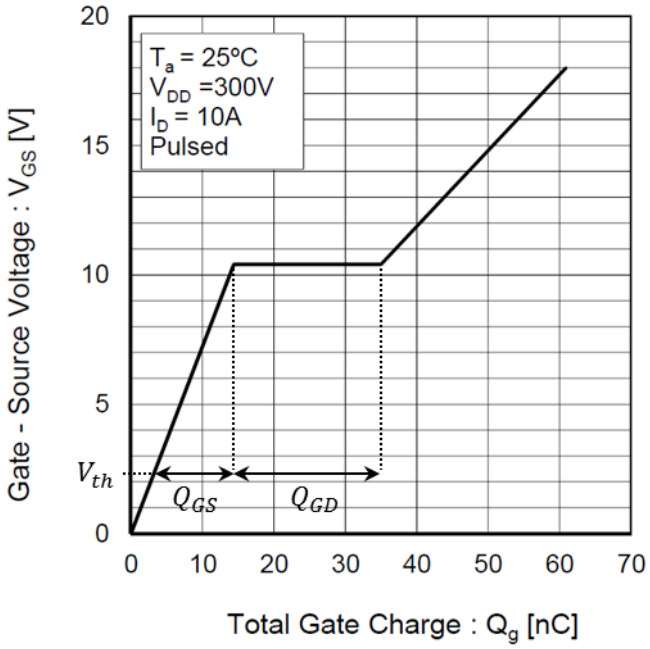


Fig. 3.5 Gate-charge profile of a ROHM SiC power MOSFET SCT2120AF [91].

3.3.2.2 Turn-off

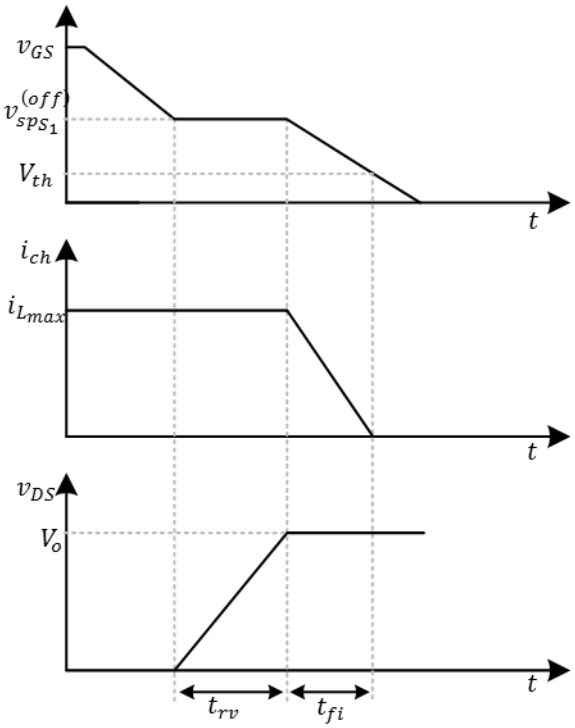


Fig. 3.6 MOSFET turn-off waveforms.

Equivalent considerations apply for the turn-off switching transient. As shown in Fig. 3.6, the switching off waveforms are specular to the turn-on ones.

After the command signal applied to the gate steps to zero, the input capacitors start discharging through a negative current i_g. The gate voltage v_{GS} starts falling, until it reaches the plateau value $v_{sp_{S_1}}^{(off)}$, which represents the minimum gate voltage required to support the full drain current $i_{DS} = I_0$. Before the diode could share the current, the drain voltage must reach $v_{DS} = V_o + V_D$, in order to positively polarize the diode. Once v_{DS} reaches its off-state value, the diode can turn on and the load current is progressively transferred from the MOSFET to the diode. Once the gate voltage falls below the threshold value V_{th}, the transition is complete.

The current i_g absorbed by the driver is assumed:

$$i_g^{(off)} = \frac{V_{dr}}{R_g} \tag{3.13}$$

Since the conduction current just before the turn off is $i_{DS_{S_1}} = i_{L_{max}}$, the *miller plateau* voltage is defined as:

$$v_{sp_{S_1}}^{(off)} = V_{th} + \sqrt{\frac{i_{L_{max}}}{\kappa_{ch}}} \tag{3.14}$$

The switching time $t_{off_{S_1}} = t_{fi} + t_{rv}$ is:

$$t_{fi} = \frac{Q_{GS}}{i_g^{(off)}}, \qquad t_{rv} = \frac{Q_{GD}}{i_g^{(off)}}, \qquad t_{off_{S_1}} = \frac{Q_{GS} + Q_{GD}}{i_g^{(off)}} \tag{3.15}$$

Then, the expression of the energy loss during turn off is:

$$E_{off}^{(MOS)} = \frac{1}{2} I_0 \, v_{DS}^{(off)} t_{off} \tag{3.16}$$

The power losses $P_{off}^{(S_1)}$ referred to the turn off transition, are evaluated as:

$$P_{off}^{(S_1)} = \frac{1}{2} i_{L_{max}} \, V_o \, t_{off_{S_1}} \, f_s \tag{3.17}$$

And similarly, for the soft switched S_2 MOSFET, the power losses $P_{off}^{(S_2)}$ are:

$$P_{off}^{(S_2)} = \frac{1}{2} i_{L_{min}} \, V_D \, t_{off_{S_2}} \, f_s \tag{3.18}$$

3.3.2.3 Intrinsic capacitors losses contribution

The periodical variation of the v_{DS} voltage from nearly zero to the reverse voltage $v_{DS}^{(off)}$ involves the charging and the discharging of the output capacitance C_{oss}. This capacitance corresponds to the sum of the drain-source and gate-drain capacitors $C_{oss} = C_{GD} + C_{DS}$ and it is provided by the manufacturer for a defined range of operating conditions. Since these capacitances depend on the width of the space-charge zones of the reverse p-n junctions in the MOSFET, their value strongly changes with the voltage applied to the terminals v_{DS}.

$$C_{oss} = C_{oss}(v_{DS}) \tag{3.19}$$

The amount of charge Q_{oss} needed to charge the output capacitor is:

$$Q_{oss} = \int_0^{v_{DS}^{(off)}} C_{oss}(v_{DS})\, dv_{DS} \tag{3.20}$$

However, the amount of charge stored when the MOSFET is in reverse state (at $v_{DS} = v_{DS}^{(off)}$), hence for $C_{oss} = C_{oss}\left(v_{DS}^{(off)}\right)$, is:

$$Q_{oss} = C_{oss}\left(v_{DS}^{(off)}\right)\, v_{DS}^{(off)} \tag{3.21}$$

In literature [33], [93], an approximated value of the power losses due to the periodical release of electric charge Q_{oss} is given by:

$$P_{C_{oss}} = \frac{1}{2} C_{oss}\left(v_{DS}^{(off)}\right) {v_{DS}^{(off)}}^2 f_s \tag{3.22}$$

in which it is assumed that the charging phase of C_{oss} is lossless.

Nevertheless, the energy stored in the intrinsic capacitor C_{GD} and C_{DS} in off-state is not entirely discharged in the MOSFET channel. This is true for C_{DS} because of its direct connection to the channel. This is partly true for C_{GD} since part of the stored energy in C_{GD} is wasted in the gate resistor R_G and the driver voltage V_{dr}. The capacitors may act like energy buffers and, to understand the energy losses, the current paths of the respective currents $i_{C_{GD}}$ and $i_{C_{DS}}$ should be carefully analysed.

As mentioned in [92], the charging/discharging currents of C_{GD} and C_{DS} flow through the hard switched MOSFET channel (S_1 in the synchronous boost case) and they are added (turn-on) or subtracted (turn-off) to the inductor current, as showed hereafter.

Fig. 3.7 depicts the switching profiles of S_1 for both turn-on and turn-off, and Fig. 3.8 indicates the related capacitors' current paths. Fig. 3.7(a) is similar to Fig. 3.3 during the period t_{ri} which corresponds to the charge of C_{GS} from V_{th} to V_{sp} (Fig. 3.8(a)) and the rise of the channel current up to i_L. Nonetheless, Fig. 3.7(a) differs from Fig. 3.3 during the period t_{fv}, i.e. as soon as the drain-source voltage v_{DS} falls. This sequence corresponds to the $C_{oss}^{(S_1)}$ discharges and $C_{oss}^{(S_2)}$ charges. Since the S_2 device is already opened (dead-band time), the capacitors currents have no choice but to flow through the S_1 channel and the converter source (Fig. 3.8(b)). This leads to a double overcurrent in the S_1 channel during the period t_{fv}. According to (3.23):

$$i_{ch} = i_{L_{min}} + 2\, i_{C_{oss}} \tag{3.23}$$

where

$$i_{C_{oss}} = i_{C_{oss}}^{(S_1)} = i_{C_{oss}}^{(S_2)} = i_{C_{GD}} + i_{C_{DS}} \tag{3.24}$$

By assuming as constant the $v_{DS}^{(S_1)}$ slope:

$$i_{C_{oss}} = \frac{Q_{oss}}{t_{fv}} \tag{3.25}$$

The power losses expression in (3.11) should be then corrected accordingly:

$$P_{on}^{(S_1)} = \left(\frac{1}{2} i_{L_{min}} V_o \, t_{ri} + \frac{1}{2}\left(i_{L_{min}} + 2\, i_{C_{oss}}\right) V_o \, t_{fv}\right) f_s \tag{3.26}$$

where the capacitors over-currents have been addressed during the period t_{fv}.

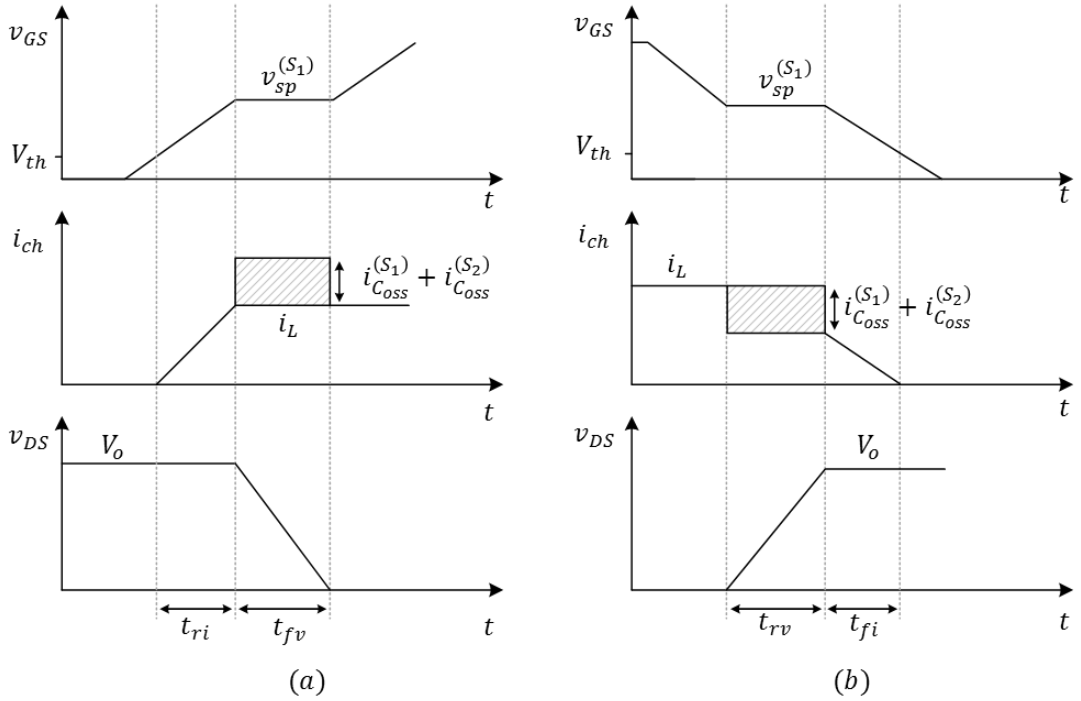


Fig. 3.7 Charging profile and switching waveforms of the S_1 turn-on (a) and turn-off (b), with the Q_{oss} contributions.

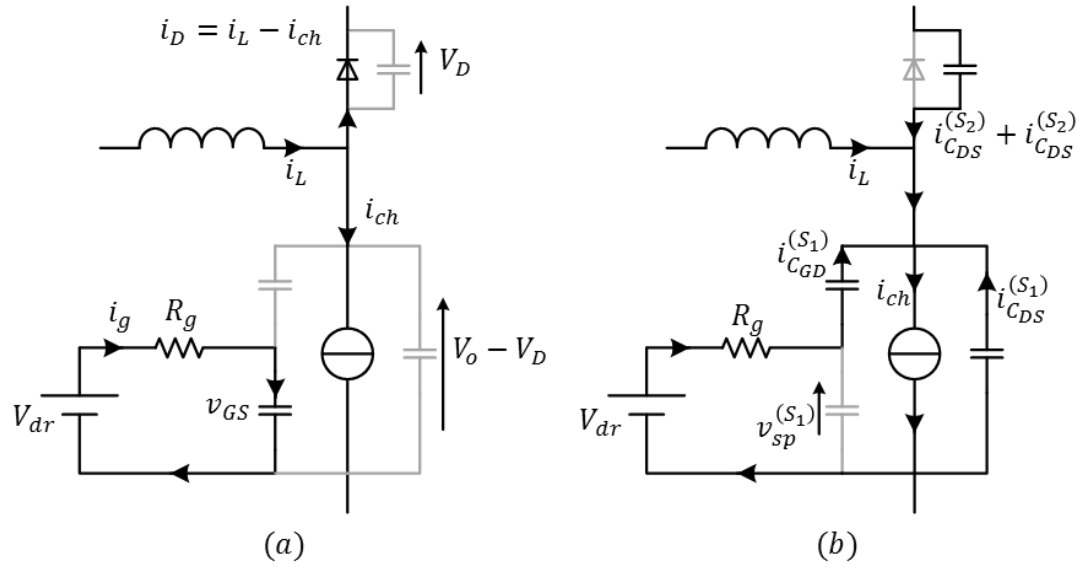


Fig. 3.8 Charging currents' paths during the periods t_{ri} (a) and t_{fv} (b) at the turn-on of S_1.

During the turn-off, the situation is reversed: the charging current through $C_{oss}^{(S_1)}$ and the discharging current through $C_{oss}^{(S_2)}$ are subtracted from the channel as depicted in Fig. 3.7(b), resulting beneficial for the power losses:

$$P_{off}^{(S_1)} = \left(\frac{1}{2}\left(i_{L_{max}} - 2\, i_{C_{oss}}\right)V_o\, \left(t_{fv} + t_{ri}\right)\right) f_s \tag{3.27}$$

3.3.3 Freewheeling Diode

The freewheeling diode D_2 intervenes during the soft switching of the switch S_2. During the dead times t_{dt} between the conduction of S_1 and S_2, it takes over the inductor current. The power losses of the diode during the two dead time periods can be expressed as:

$$E_{D_2}^{(dt)} = V_D\, i_{L_{min}} t_{dt} + V_D\, i_{L_{max}} t_{dt} = 2\, V_D\, I_L\, t_{dt} \tag{3.28}$$

An important contribution to the power losses through the diode is brought by the reverse recovery phenomenon: when the MOSFET S_1 starts conducting, the charge Q_{rr} removed from the p-n junction of the body diode D_2 flows into the S_1 channel. A great amount of Q_{rr} causes an over peak of the current through S_1, which can be potentially dangerous for the reliability of the device. Due to the features of the wide bandgap materials, the recovery power loss in SiC devices is reduced to a fraction of a few to tens of percentiles compared to a body diode of a Si-MOSFET or to the Si fast recovery diode employed with IGBTs as freewheeling diode. The reverse recovery charge depends on several factors such as the current conducted by the diode and its slope di_D/dt during the turn off. Besides, a Schottky diode is often employed for the freewheeling function, which does not exhibit any recovery charge because of its unipolar nature.

The reverse recovery data (usually Q_{rr}, the recovery time t_{rr}, the diode reverse current peak I_{rr} or the recovery energy E_{rr}) are available just at the operating point provided by the manufacturer. Nevertheless, for wide bandgap devices, the impact of the reverse recovery energy on the power losses can be considered not very influencing, hence the reverse recovery charge value Q_{rr} can be assumed as the one reported on the device datasheet, and the relative power losses can be approximated to:

$$P_{D_2}^{(rr)} = \frac{1}{2}\, Q_{rr}\, v_{DS_{S_2}}^{(off)}\, f_s \tag{3.29}$$

3.3.4 Thermal analysis

The thermal management of the internal temperature of the semiconductor device is a mandatory step in the design procedure of a power electronic system. At high temperatures, the density of the minority carriers in the most slightly doped region of the device equals the majority carriers' density. Such increase of the intrinsic carriers short out the built-in potential barrier in the depletion region of the junction, which lose its rectifying function [31]. This condition is highly undesirable and disruptive; hence the manufacturers usually provide temperature ratings largely smaller than the critical one (intrinsic temperature). Even if the semiconductor junction does not reach the critical temperature, the continual operation at high temperature compromises the reliability and the life-time of the semiconductor device, possibly of the entire converter [93].

In order to evacuate the heat produced by the energy waste and handle the semiconductor temperature, a cooling system should be integrated in the converter. The heat path from the junction to the environment strongly depends on the arrangement of the board and the integration level of the system. In the considered case, the power device is directly mounted on an aluminium heatsink. The device case and the heatsink are connected through a thermal interface material (TIM), which is a thermal conductor

(the electrical insulation, if required, depends on the material). The TIM considered in the design is a thermal grease, which has the best thermal conductivity but have higher thermal resistance at the contact surfaces. To contain the thermal resistance, it requires a mounting mechanism that keeps constant pressure between the heat sink and the device. Fig. 3.9(a) shows the heat path through the cross section of the system composed of the device and the cooling system. The relationship between the temperature along the path, the power losses of the device and the thermal resistance can be modelled by an equivalent circuit in Fig. 3.9 (b).

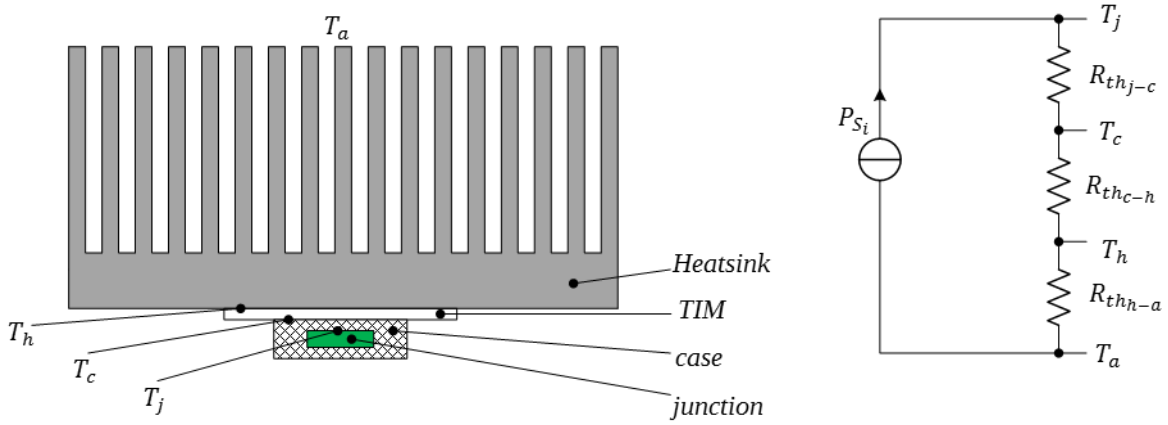


Fig. 3.9 Heatsink cross section (a) and equivalent thermal circuit (b).

The resulting junction temperature, with P_{S_i} the power losses of the i^{th} device, is:

$$T_j = \left(R_{th_{h-a}} + R_{th_{j-c}} + R_{th_{c-h}}\right) P_{S_i} + T_a \tag{3.30}$$

where T_a represents the ambient temperature, $R_{th_{h-a}}$ is the thermal resistance from the heatsink surface to the environment, $R_{th_{j-c}}$ is the thermal resistance from the junction to the device's case and $R_{th_{c-h}}$is the thermal resistance of TIM. $R_{th_{j-c}}$ and $R_{th_{c-h}}$ clearly depend on the device package and TIM material. Whereas $R_{th_{j-c}}$ is available in the semiconductor device datasheet, $R_{th_{c-h}}$ can be obtained as:

$$R_{th_{c-h}} = \frac{t_{TIM}\, \varrho_{TIM}}{A_{c-h}} \tag{3.31}$$

where t_{TIM} is the thickness of the TIM layer, ϱ_{TIM} is its thermal resistivity and A_{c-h} is the contact surface between heatsink and the device case.

3.3.4.1 Temperature effect on the MOSFET parameters

As already mentioned, semiconductor devices parameters change with the temperature variation and their performances are affected as well. The manufacturer shows the dependency of the MOSFET characteristics as function of the temperature. Namely, they often provide the temperature influence on the channel resistance r_{DS} and the threshold voltage V_{th}. Furthermore, the trans-conductance characteristic i_{DS}-v_{GS} has a remarkable variation with the junction temperature, as shown in Fig. 3.4. It leads to a variation of the parameters related to this characteristic, as the trans-conductance value g_{f_s} or, in the considered case, the factor κ_{ch} introduced in (3.7). The temperature dependency of the mentioned parameters is assumed linear and expressed as [94]:

$$r_{DS} = r_{DS}|_{@25°C}\left(1 + \rho_{T_j}(T_j - 25°C)\right) \tag{3.32}$$

$$V_{th} = V_{th}|_{@25°C}\left(1 + \nu_{T_j}(T_j - 25°C)\right) \tag{3.33}$$

$$\kappa_{ch} = \kappa_{ch}|_{@25°C}\left(1 + \varsigma_{T_j}(T_j - 25°C)\right) \tag{3.34}$$

where ρ_{T_j}, ν_{T_j} and ς_{T_j} are the temperature coefficients respectively of the values r_{DS}, V_{th} and κ_{ch}. Taking into account the temperature effect in the evaluation of the MOSFET power losses, the expression in (3.30) becomes:

$$T_j = \left(R_{th_{h-a}} + R_{th_{j-c}} + R_{th_{c-h}}\right) P_{S_i}\left(r_{DS}(T_j), V_{th}(T_j), \kappa_{ch}(T_j)\right) + T_a \tag{3.35}$$

If the heatsink has been selected and its thermal resistance is already known, the implicit equation (3.35) can be numerically solved, since the relation between the temperature T_j and the power losses is strongly non-linear. An example of an iterative loop for the research of the junction temperature T_j is shown in the following Fig. 3.10.

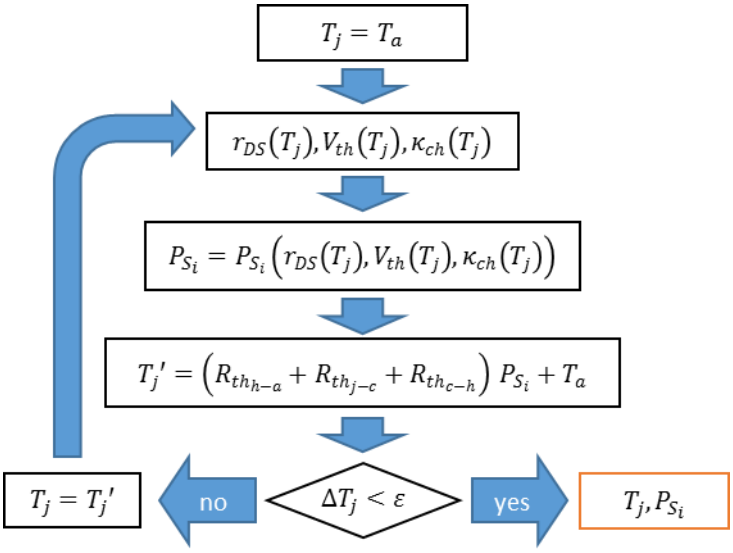


Fig. 3.10 Thermal cycle flowchart example for the evaluation of the MOSFET losses (fixed $R_{th_{j-a}}$).

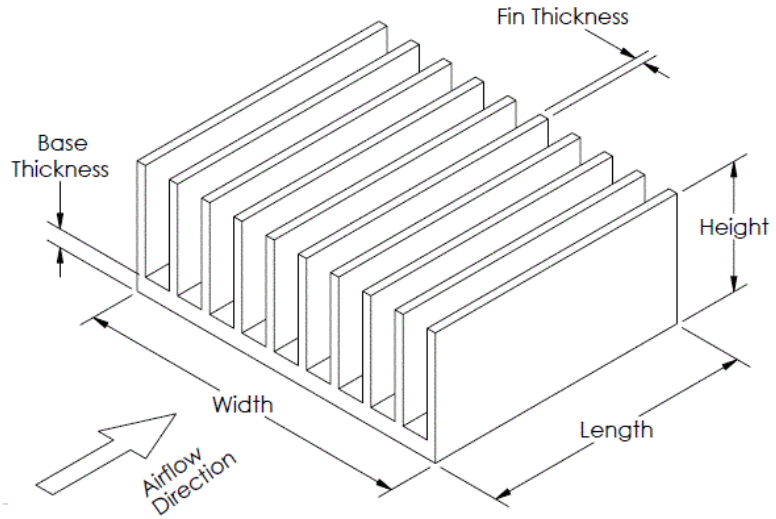
Such algorithm is a tool to verify the power device suitability. Once the convergence criteria are met, if the T_j value obtained is smaller than the temperature rating reported by the datasheet, the selected device is suitable for the task. The T_j value can also provide an important information concerning the fitness of the device with the application. If, for example, the junction temperature value T_j is too close to the environment temperature T_a, then the device is underused, and a component with lower ratings (and probably cheaper) would likely be sufficient.

If the objective of the thermal analysis is to choose a suitable heatsink, a common way to proceed consists into assuming the junction temperature in the worst case, then at the maximal permissible value allowed $T_{j_{MAX}}$. The power dissipated by the semiconductor is evaluated accordingly, and the required thermal resistance is deducted from (3.35):

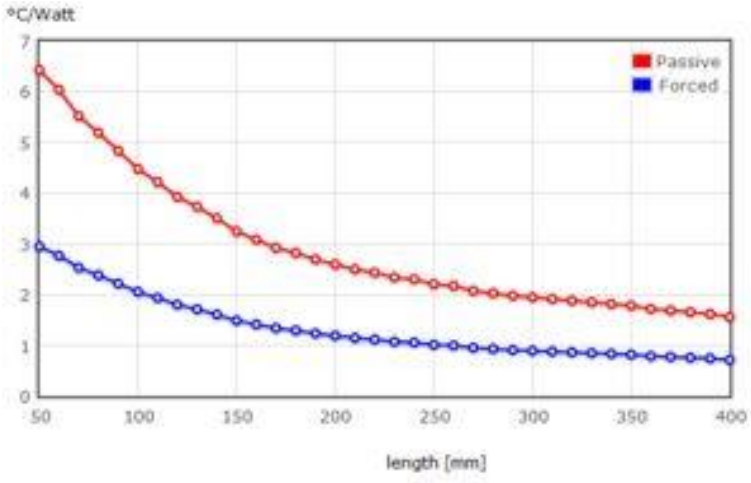
$$R_{th_{h-a}} = \frac{\left(T_{j_{MAX}} - T_a\right)}{P_{MOS}\left(r_{DS}\left(T_{j_{MAX}}\right), V_{th}\left(T_{j_{MAX}}\right), \kappa_{ch}\left(T_{j_{MAX}}\right)\right)} - R_{th_{j-c}} - R_{th_{c-h}} \tag{3.36}$$

3.3.4.2 Heatsink design

The cooling system contributes to a large proportion of the converter volume and mass. A common way to characterize the thermal resistance $R_{th_{h-a}}$ of a heatsink is to solve the thermodynamic equations related to its specific geometry and material [95]. A finite elements analysis tool could perform these calculations with good accuracy, but it requires a high computational complexity. A more suited approach consists into using the information provided by the heatsinks manufacturer in order to relate the required thermal resistance $R_{th_{h-a}}$ with the heatsink size [96], [97]. In this study, to ease the selection among the existing components, the latter option has been preferred.



(a)



(b)

Fig. 3.11 Extruded heatsink geometry (a) and thermal resistance $R_{th_{h-a}}$ values as function of the heatsink length [98].

The considered cooling system consists of an extruded heatsink. Once the fin geometry of the extruded heatsink has been chosen, hence the heatsink cross-section (Fig. 3.11 (a)), the manufacturer provides the thermal resistance values for different lengths l_h (then volume) and different values of the coolant's flow rate in case of forced convection [98]. Usually, the thermal resistance values should be multiplied by a temperature factor provided by the heatsink manufacturer [99], which considers the relation between thermal resistance and temperature excursion $\Delta T = T_h - T_a$. By fitting the thermal resistance values $R_{th_{h-a}}$ provided in the datasheet, it is possible to obtain an exponential relation between the heatsink volume $V^{(heatsink)}$ and the required thermal resistance $R_{th_{h-a}}$:

$$V^{(heatsink)} = z_h \left(R_{th_{h-a}}\right)^{p_h} \tag{3.37}$$

where z_h and p_h are fitting parameters. This approach is simple, but it could be inaccurate. Then it should be considered as a pre-sizing method. The normal functioning should be validated on the test bench.

3.4 Passive Components

3.4.1 Magnetic component design

Table 3.2 Inductor parameters.

Symbol	Description
L	Inductance value
n_L	Turns number
A_{core}	Magnetic Core section
MLT_L	Mean length per turn
W_A	Winding area
l_m	Magnetic mean path length
μ_r	Relative permeability of the magnetic core
μ_0	Magnetic permeability in the air

The inductor design, even if considered individually, presents several degrees of freedom. A simple model of the inductor is described as:

$$v_L(t) = L\frac{di_L(t)}{dt} - DCR_L\, i_L \cong L\frac{\Delta i_L}{\Delta t} \tag{3.38}$$

Instantaneous voltage v_L and current i_L across the inductor are related as in (3.38), where L is the inductance value and DCR_L is the series resistance through the windings. In a SMPS, the magnetic energy is stored and released depending on the configuration of the circuit.

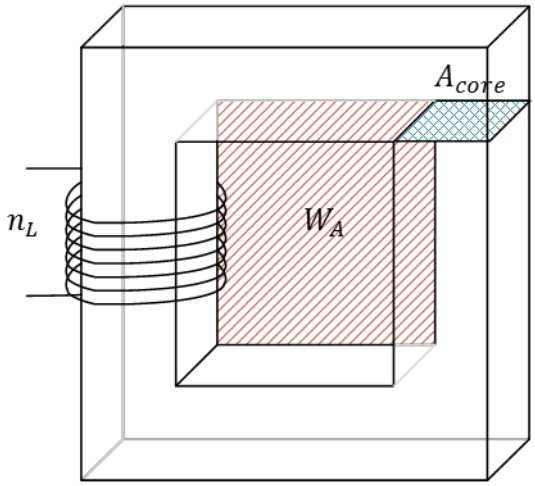


Fig. 3.12 Simplified inductor shape.

During each configuration (operating sequence) of the converter, the voltage v_L assumes an almost constant value (the ripple voltage across the capacitor is supposed negligible), positive in the charging phase (V_{in} in a boost converter, Fig. 3.2), negative in the discharging (V_o in a boost converter, Fig. 3.2). If the time constant $\tau_L = L/DCR_L$ of the solution of the differential equation (3.38) is larger enough than the converter switching period T_s ($\tau_L \gg T_s$), the current derivative di_L/dt during each converter sequence can be approximated as the ratio between the peak-to-peak current ripple Δi_L and the duration Δt of the considered sequence of the converter ($di_L/dt \cong \Delta i_L\ /\Delta t$).

The value of inductance L depends on the magnetic core material and shape, as well as the number of coils n_L. In (3.39), the reluctance $\Re_L$ is determined from the mean magnetic path length l_m, the magnetic core section A_{core} (Fig. 3.12) and the relative magnetic core permeability μ_r.

$$L = \frac{n^2}{\Re_L}, \qquad \Re_L = \frac{l_m}{A_{core}\ \mu_0\ \mu_r} \tag{3.39}$$

At the end of the charging phase, the inductor current, and then the magnetic flux in the magnetic core, reach the maximum value. This moment defines the maximum magnetic energy stored by the inductor in steady state:

$$E_L = \frac{1}{2} L\ i_{L_{max}}^2, \qquad i_{L_{max}} = < i_L >_{T_s} + \frac{\Delta i_L}{2} = I_L + \frac{\Delta i_L}{2} \tag{3.40}$$

This quantity is an important parameter in the inductor design, since the size and weight of the inductor core depends strictly on the stored energy [100], then on the value of inductance and on the maximal current.

The following equations represent the basic magnetic laws (Lenz's law, Ampere's law and constitutive laws) for a solenoid with the assumption of an isotropic and linear magnetic core [33]:

$$v_L(t) = n_L \frac{d\Phi_L}{dt} \tag{3.41}$$

$$n_L i_L = \oint H_L\ dl = H_L l_m \tag{3.42}$$

$$B_L = \mu_0 \, \mu_r H_L \tag{3.43}$$

$$\Phi_L = \oiint B_L \, dA = A_{core} \, B_L \tag{3.44}$$

From the equations above, the stored energy can be expressed as:

$$E_L = \frac{1}{2} L \, i_{L_{max}}^2 = \frac{A_{core} \, \mu_0 \, \mu_r}{2 \, l_m} \left(\frac{B_{L_{max}} \, l_m}{\mu_0 \, \mu_r \, n} \right)^2 \tag{3.45}$$

which can be reduced to:

$$E_L = \frac{B_{L_{max}}^2}{2 \, \mu_0 \, \mu_r} A_{core} l_m = \frac{B_{L_{max}}^2}{2 \, \mu_0 \, \mu_r} \, V_{core} \tag{3.46}$$

where V_{core} is the magnetic core volume. Equation (3.46) provides the approximate minimum value of the magnetic core V_{core}, evaluated while working with a magnetic flux density close to the saturation:

$$V_{core} = \frac{2 \, \mu_0 \, \mu_r}{B_{sat}^2} E_L = \frac{\mu_0 \, \mu_r}{B_{sat}^2} \, \frac{V_i D}{\Delta i_L \, f_s} \left(< i_L >_{T_s} + \frac{\Delta i_L}{2} \right)^2 \tag{3.47}$$

In (3.47), the switching frequency f_s contributes to the current ripple amplitude Δi_L, hence on the maximal current value $i_{L_{max}}$ and the magnetic field through the core. It is clear that a high switching frequency allows reducing either the required inductance value or the magnetic flux through the core. In both cases, a smaller inductor core can be chosen. Moreover, in (3.47), a particular emphasis has been given to the dependency from the inductance current ripple Δi_L. Its value (which depends from the inductance L and the switching frequency f_s as in Table 3.1) not only affects the power losses and the size of the inductor, but it also affects performances and design of the other components as well. Moreover, the semiconductor devices current ratings need to be opportunely chosen in order to sustain the inductor maximal current. A large ripple current leads to the choice of semiconductor devices with higher current ratings, which have a higher price and usually exhibits poorer dynamical performances in commutation. Furthermore, the DM input filter shall provide the necessary attenuation for the rejection of the input current harmonic at the switching frequency. The harmonic content magnitude depends on the ripple Δi_L, determines, along with the switching frequency, the size of the filter. Similar consideration can be made about the impact of the inductance value L instead.

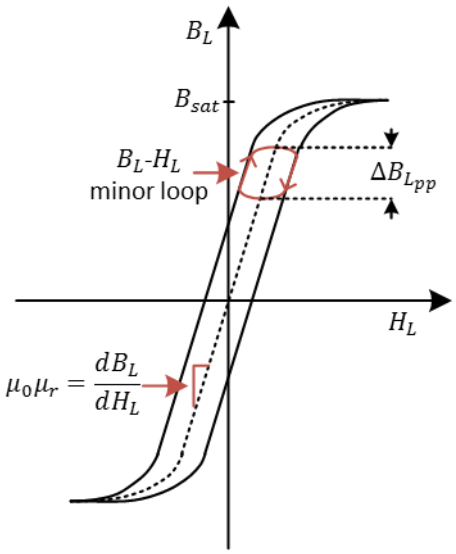
3.4.1.1 Magnetic saturation

The relationship between the magnetic field H_L and the magnetic flux density B_L within a magnetic core is strongly non-linear. As shown in Fig. 3.13(a), it exhibits both hysteresis and saturation. The permeability decreases with the magnetic field intensity H_L, as shown in Fig. 3.13(b).

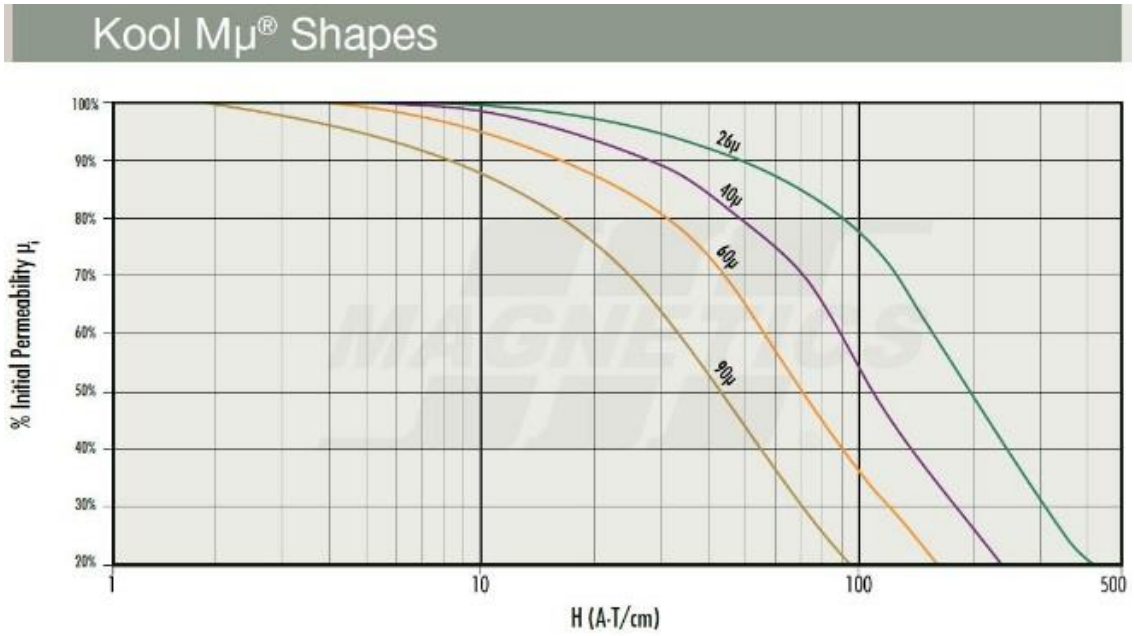
In the common approach, the inductor is designed to work at high permeability values, then below the saturation flux density B_{sat}:

$$n_L \frac{i_{L_{max}} \, \mu_0 \, \mu_r}{l_m} < B_{sat} \tag{3.48}$$

In case of saturation, the impedance abruptly decreases and the inductor behaves like a short circuit.



(a)



(b)

Fig. 3.13 B-H characteristic in a magnetic core (a) and magnetic permeability decay with the magnetic field H [101] (b).

To decrease the flux density, one could think to reduce the number of windings n_L, but, below a certain value of n_L, the $i_{L_{max}}$ term in (3.48) increases because of the high current ripple Δi_L, which lead to saturation of the core, as shown in Fig. 3.14. The material permeability can be tuned in order to lower the magnetic flux density and prevent the saturation. A common way to decrease the permeability value is to add an air gap in the magnetic path. In this way, the equivalent relative magnetic permeability μ_{eq} can be set as follow:

$$\mu_{eq} = \frac{\mu_r \, l_m}{l_{gap} \, \mu_r + l_m} \tag{3.49}$$

where l_{gap} is the air-gap thickness. In this way, the B-H characteristic slope is decreased, and the magnetic field saturation $H_{L_{sat}}$ value is increased, along with the saturation current:

$$H_{L_{sat}} = n_L \frac{i_{L_{sat}}}{l_m} \tag{3.50}$$

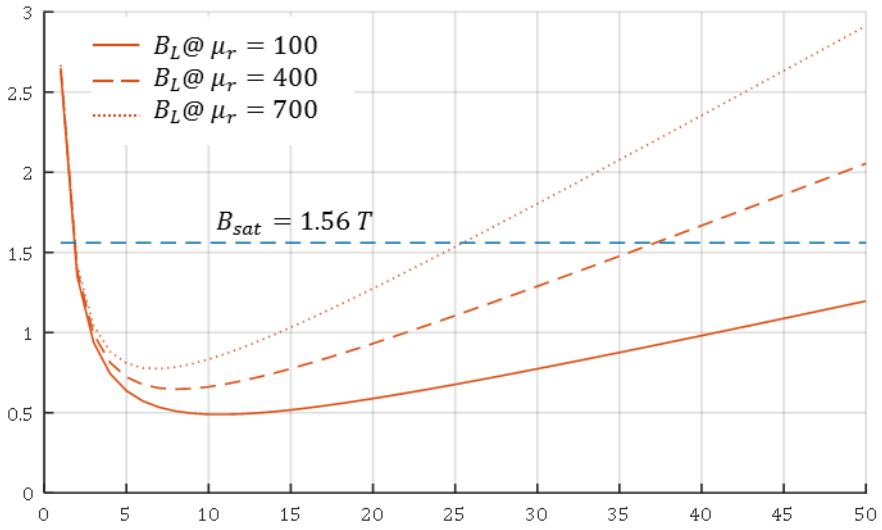


Fig. 3.14 Magnetic induction B_L in a magnetic core AMCC 0063 Hitachi Metglas [102] as function of the turns number n_L and the permeability value μ_r.

This technique is employed especially with high permeability materials, like ferrite ones. The proper assembling of the different parts of the core as well as setting the right air gap could always lead to some imperfections and discrepancies in regards with the expected permeability value.

In SMPS, distributed powder cores are widely used too. These materials present several advantages, like high resistivity, low hysteresis and eddy current losses and excellent inductance stability over wide temperature and frequency ranges.

Both solutions, for the same value of inductance L, inevitably lead to a bulkier core with a larger section A_{core}. On top of that, the power losses due to the magnetic field hysteresis are more significant.

In this work, the second solution was preferred. The magnetic cores used are powder cores produced by Magnetics. Namely, two types of magnetic cores have been employed. The MPP cores have been used for the realization of the input filter inductor L_{fil}. As mentioned in the Magnetics website [103], Molypermalloy Powder (MPP) cores, are distributed air gap cores made from a 79% Nickel, 17% Iron, and 4% Molybdenum alloy powder, recommended for the lowest core losses of any powder core material. The MPP material has been preferred for the high stability of its magnetic permeability at high frequencies.

For the realization of the boost inductor L, High Flux powder cores were employed as candidates. As mentioned in the Magnetics website [104], the Magnetics High Flux cores are distributed air gap cores made from a 50% Nickel and 50% Iron alloy powder, recommended for the highest available biasing capability of any powder core material. Indeed, for this material, the flux density saturation limit is relatively high ($B_{sat} = 1.5\ T$) and it exhibits low core losses. These properties make this type of magnetic core an appropriate candidate for the realization of the boost inductor L (both a smaller magnetic core and a large flux density are required).

3.4.1.1.1 DC Bias Permeability dependency

From the non-linear relationship between the magnetic field strength H_L and the magnetic flux density B_L, as shown In Fig. 3.13, we observe that the magnetic permeability is not a constant value, but decreases along with the magnetic field. For H_L values close to the saturation level, the inductance value, then the inductor impedance, strongly decreases. The permeability roll-off may be steep or smooth depending on the core material. The rate of decay of inductance/permeability as function of the DC current value is smoother for powdered iron core inductors, especially if compared to the ferrite-based ones [105]. The inductor is usually designed in order to work within the linear B-H operating zone, where the permeability value is almost constant. Imposing the inductor to operate in low-saturation region involves that the magnetic core of the component has to be oversized, or the relative permeability reduced, in order to limit the magnetic field strength below a certain limit. As shown in [106], more compact design solutions can be obtained with inductors which operates close to the saturation.

Often, the manufacturer provides the roll-off factor k_{DC} as function of the magnetic field strength H_L. This coefficient shall be taken into account in the evaluation of the real value of inductance:

$$L = \frac{n_L^2}{\mathfrak{R}_L}\, k_{DC}(H_L), \qquad H_L = \frac{n_L\, i_L}{l_m} \tag{3.51}$$

3.4.1.2 Series resistance

Furthermore, others feasibility factors shall be considered. The n number of coils is practically limited by the winding area W_A (refer to Fig. 3.12). The number of coils, along with the copper wire section and the core section perimeter, define the resistance of the windings:

$$DCR_L = \frac{\rho_{cu}\, n_L\, MLT_L}{A_{wire}} \tag{3.52}$$

where ρ_{cu} is the copper resistivity, MLT the perimeter of the core section A_{core} and A_{wire} is the wire cable section. Equation (3.52) takes into account the resistance value just for low frequency current harmonics. At higher frequencies, the effective wire section decreases because of the eddy currents and the skin effect. The penetration depth δ_w of the current through a wire is given by:

$$\delta_w = \sqrt{\frac{\rho_{cu}}{\pi\, \mu_0\, f}} \tag{3.53}$$

The wire section is then reduced to a ring whose section is defined as:

$$A'_{wire} = \pi\, \delta_w\, (d_w - \delta_w) \tag{3.54}$$

where d_w is the wire cable diameter. Then, the DCR_L resistance increases with the frequency because the effective wire section A'_{wire} reduction. In case of more windings layers, proximity effect shall be considered too [33]. The copper losses are given by the sum of the contribution of each harmonic of the i_L current and the resistance value evaluated at the respective frequency:

$$P_L^{(copper)} = \sum_{i=0} DCR_L^{(i)}\, \left(i_L^{(i)}\right)^2 \tag{3.55}$$

where $DCR_L^{(i)}$ is the copper resistance at the i^{th} harmonic frequency and $i_L^{(i)}$ is the i^{th} harmonic of the inductor current i_L. In DC/DC power supplies, the DC harmonic (mean value) is usually largely superior

to the others. A reasonable approximation consists into splitting the power losses in a DC term and an AC term as:

$$P_L^{(copper)} = DCR_L^{(DC)}\, I_L^2 + DCR_L^{(AC)} \sum_{i=1} \left(i_L^{(i)}\right)^2 = DCR_L^{(DC)}\, I_L^2 + DCR_L^{(AC)} \left(i_{L_{rms}}^{(AC)}\right)^2 \tag{3.56}$$

In (3.56), the term $i_{L_{rms}}^{(AC)}$ represents the RMS value of the AC component of the i_L current and the values $DCR_L^{(DC)}$ and $DCR_L^{(AC)}$ represent respectively the series resistance evaluated for the two main harmonics of the inductor current i_L ($f = 0$ and $f = f_s$).

The power losses due to the Joule effect can then be approximated to:

$$P_L^{(copper)} = DCR_L^{(DC)}\, I_L^2 + DCR_L^{(AC)} \left(\frac{\Delta i_L^2}{12}\right) \tag{3.57}$$

3.4.1.3 Core Power losses

The energy storage and release in the magnetic core does not come without costs. Besides the power losses due to the resistance in the windings, a certain amount of power is wasted due to the periodical magnetization of the core. The area encircled by the B-H minor loop in a switching cycle, shown in Fig. 3.13(a), represents the amount of wasted energy per volume unit defined as:

$$\varepsilon_L^{(core)} \left[\frac{J}{m^3}\right] = \oint H_L\, dB_L \tag{3.58}$$

Due to the cores conductivity, the alternative magnetic flux induces eddy currents within the material itself, which bring additional core losses.

The power losses in a magnetic core are commonly conceived as the sum of the two latter effects. The analytical characterization of the power losses was introduced in [107], [108], expressed as follows by the Steinmetz equation (after Charles P. Steinmetz):

$$P_L^{(core)} = A_{core}\, l_m\, k_{fe}\, f_I^{\alpha} \left(\frac{B_L|_{f=f_I}}{2}\right)^{\beta} \tag{3.59}$$

$$B_L(t) = n_L\, \mu_0\, \mu_r\, \frac{i_L(t)}{l_m} \tag{3.60}$$

where f_I and $B_L|_{f=f_I}$ are respectively the frequency and the magnitude of the first harmonic (in a DC/DC converter $f_I = f_s$) of the magnetic field density $B_L(t)$. The material parameters k_{fe}, α and β are accordingly referred as Steinmetz parameters, which are often provided by the manufacturers in the datasheet. This law is empirical and valid just for a limited frequency and flux density ranges and for sinusoidal excitations. This represents a major drawback since, in most power electronics applications, the inductors cores work with non-sinusoidal flux waveforms.

The aforementioned limitations are currently investigated to extend the solution to non-sinusoidal problems.

The MSE (Modified Steinmetz Equations) approach [109] improved the losses model by adding a term to include the dependency from the weighted time variation of the magnetic field in the core dB_L/dt. The limitation of this model lies in the arbitrary assumption about the averaging method to deduce an equivalent operating frequency [110], [111].

The generalised Steinmetz equations (GSE), developed in [112], aims to solve some MSE inaccuracies concerning the frequency dependency of the power losses, but many results showed that it could be even more inaccurate than MSE in some conditions [78].

In [113], the GSE were improved (iGSE) and a method to deal with minor hysteresis loops was developed. The iGSE is currently a widely used approach, since it provides satisfying results with any flux waveform, without any additional parameter extraction. The expression of the iGSE for a single loop is:

$$P_L^{(core)} = V_{core}\ \frac{1}{T_s}\int_0^{T_s} k_i \left|\frac{dB_L}{dt}\right|^{\alpha} \Delta B_{L_{pp}}^{\beta-\alpha}\ dt \tag{3.61}$$

where the coefficient k_i is deduced by equalizing the losses expressed in (3.61) to the Steinmetz equations in (3.59), in case of pure sinusoidal magnetic field:

$$k_i = \frac{k_{fe}}{(2\pi)^{\alpha-1}\int_0^{2\pi}|\cos\theta|^{\alpha}\ 2^{\beta-\alpha}\ d\theta} \tag{3.62}$$

Nevertheless, this model still raises some issues in regards to the selection of the appropriate parameters for Steinmetz equations. Indeed, the DC magnetization and the frequency effects on the Steinmetz parameters in different magnetization loops are not addressed.

In a boost converter, the single magnetization loop at f_s shall be considered. Equation (3.61) becomes:

$$P_L^{(core)} = V_{core}\ \ k_i\ \Delta B_{L_{pp}}^{\beta-\alpha}\left(\left(\Delta B_{L_{pp}}\frac{f_s}{D}\right)^{\alpha} D + \left(\Delta B_{L_{pp}}\frac{f_s}{D'}\right)^{\alpha} D'\right) \tag{3.63}$$

where

$$\Delta B_{L_{pp}} = n_L\ \mu_0\ \mu_r\ \frac{\Delta i_L}{l_m} \tag{3.64}$$

It is clear that the volume and the switching frequency have both a role in determining the core losses of the inductor. By developing (3.63) and (3.64), it is possible to highlight a clearer dependence from the switching frequency f_s:

$$\begin{aligned} P_L^{(core)} = V_{core}\ k_i \left(n_L\ \mu_0\ \mu_r V_i \frac{D}{f_s L\ l_m}\right)^{\beta-\alpha} \left(\left(n_L\ \mu_0\ \mu_r\ \frac{V_i}{l_m L\ D'}\right)^{\alpha} D \right. \\ \left. + \left(n_L\ \mu_0\ \mu_r\ V_i \frac{D}{l_m L\ D'}\right)^{\alpha} D'\right) \end{aligned} \tag{3.65}$$

In conclusion, for high switching frequencies, a smaller core can be selected, since the inductor needs to store a smaller magnetic energy. The frequency f_s appears under the exponent $-\beta+\alpha$, hence the materials properties. Usually $\alpha \in [1,2]$ and $\beta \in [2,3]$, hence a difference $\beta-\alpha<1$ leads to a beneficial contribution of higher frequencies.

3.4.2 Output Capacitor

The role of the output capacitor C_o consists into maintaining the output voltage constant as much as possible by filtering the current supplied by the switch S_2. Due to the discontinuous nature of this current, the capacitance value results pretty high. The design of the output capacitor is strictly related to the

voltage requirements $\Delta v_{o_{lim}}$ at the output terminals. The nominal voltage ripple Δv_o depends on the C_o capacitance value and ripple of the electric charge ΔQ_{C_o} absorbed by the capacitor, defined in the previous chapter. A large capacitance value allows reducing the amplitude of the voltage ripple, but it causes a larger amount of stored energy $E_C = 0.5\ C\ V_o^2$. Indeed, the size of the capacitor itself is related, besides to the capacitor technology and brand, to the rated stored energy [114]. Fig. 3.15 shows the data provided by the Vishay manufacturer for different voltages ratings of the MKP series [115]; the volume of film capacitors increases linearly with the rated electrostatic energy.

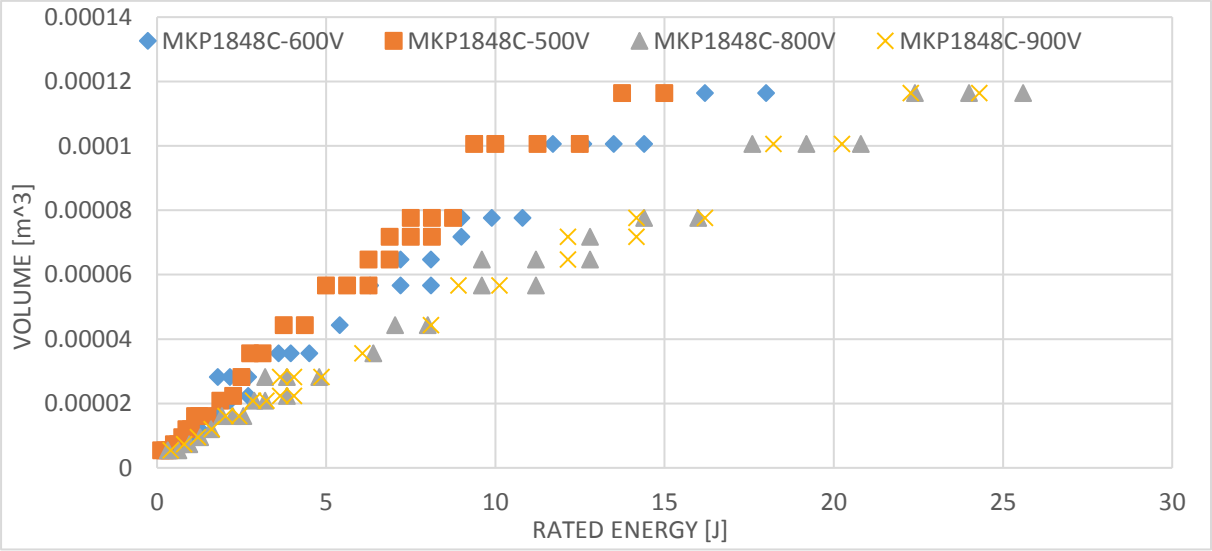


Fig. 3.15 Stored energy ratings of Vishay MKP series capacitors [115], for different voltage ratings.

As for the inductor, a higher switching frequency helps reducing the capacitance value.

In the case of a boost converter, in steady state, the current through the capacitor is discontinuous because of the switch S_2.

In Fig. 3.16, the L inductor and the C_o capacitor current waveforms are showed in steady state operation.

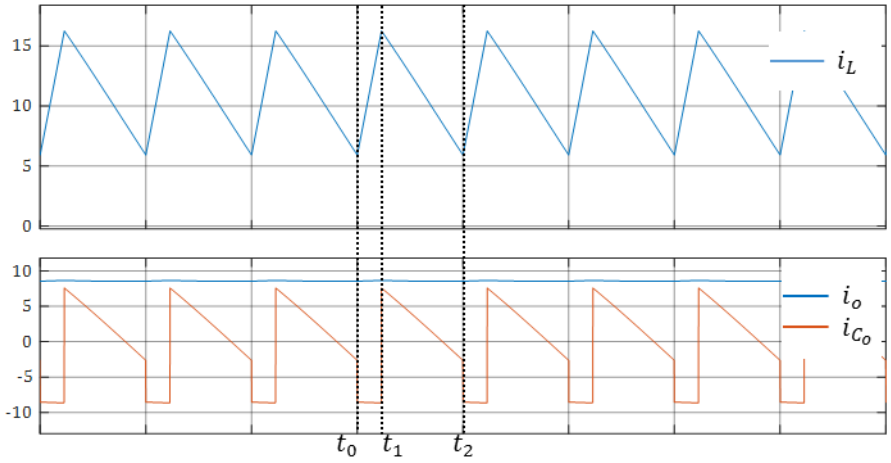


Fig. 3.16 Steady state i_L and i_{C_o} waveforms ($L = 300\mu H, C_o = 22\mu F, f_s = 20kHz, V_o = 350V, P_o = 3kW, V_{in} = 270V$).

Two configurations ($u = 0$ or $u = 1$) occurs within a switching period $T_s = [t_0, t_2]$. The analytical expressions of the inductor and capacitor current waveforms (shown in Fig. 3.16) are given:

$$\begin{cases} i_L = I_L - \Delta i_L \left(\frac{1}{2} - \frac{(t - t_0) f_s}{D} \right) & t \in [t_0, t_1], u = 1 \\ i_{C_o} = -I_o \end{cases} \tag{3.66}$$

$$\begin{cases} i_L = I_L + \Delta i_L \left(\frac{1}{2} - \frac{(t - t_1) f_s}{D'} \right) & t \in [t_1, t_2], u = 0 \\ i_{C_o} = -I_o + i_L \end{cases} \tag{3.67}$$

The following analysis are performed under the assumption of a pure capacitive impedance. In the first period $[t_0, t_1]$, the capacitor C_o delivers an almost constant current to the load. The voltage v_{C_o} expression depends on the integral of the current through C_o:

$$v_{C_o}(t) = v_{C_o}(t_0) + \frac{1}{C_o} \int_{t_0}^{t} i_{C_o}(\tau) d\tau \tag{3.68}$$

The voltage v_{C_o} clearly reaches its minimum value at the end of the discharging sequence $t_1 = D\, T_s$ as shown in Fig. 3.17:

$$v_{C_{o\,min}} = v_{C_o}(t_1, C_o) \tag{3.69}$$

As shown in [116], to determine the maximum value of v_{C_o} during the interval $[t_1, t_2]$, two cases should be considered. If the capacitor current i_{C_o} falls to zero before the end of the switching period ($t = t_2$), v_{C_o} reaches its maximum value at t_2' within the interval $[t_1, t_2[$ (Fig. 3.17(a)); the value of t_2' is found from (3.67) by setting $i_{C_o} = 0$. Otherwise, v_{C_o} reaches its maximum value at t_2 (Fig. 3.17(b)). The limit condition between the two cases is determined by the slope of the inductor current in the discharging phase di_L/dt, hence the operating point (output/input voltages and load power), the switching frequency f_s and the inductance value L.

The limit condition is given by:

$$L_{lim} = \frac{V_{in}^2}{2 f_s P_o} \tag{3.70}$$

For the case depicted in Fig. 3.17, $L_{lim} = 600 \mu H$.

Depending on the inductance value L, the maximal voltage $v_{C_{o\,max}}$ changes:

$$v_{C_{o\,max}} = \begin{cases} v_{C_o}(t_2') & L < L_{lim} \\ v_{C_o}(T_s) & L > L_{lim} \end{cases} \tag{3.71}$$

The minimal C_o value which ensures keeping the output voltage ripple within its specification limit $\Delta v_{o_{lim}}$ in steady-state is found by the following equation:

$$\Delta v_{C_o}^{(steady)}(C_o) = \left| v_{C_{o\,max}} - v_{C_{o\,min}} \right| < \Delta v_{o_{lim}} \tag{3.72}$$

where $v_{C_{o_{max}}}$ and $v_{C_{o_{min}}}$ are expressed as function of C_o. The C_o solutions to (3.72) in the two mentioned cases are:

$$C_o = \begin{cases} D' \dfrac{\left(I_L - I_o + \dfrac{\Delta i_L}{2}\right)^2}{2\,\Delta i_L\,\Delta v_{o_{lim}}\,f_s} & L < L_{lim} \\ D' \dfrac{(I_L - I_o)}{2\,\Delta v_{o_{lim}}\,f_s} & L > L_{lim} \end{cases} \tag{3.73}$$

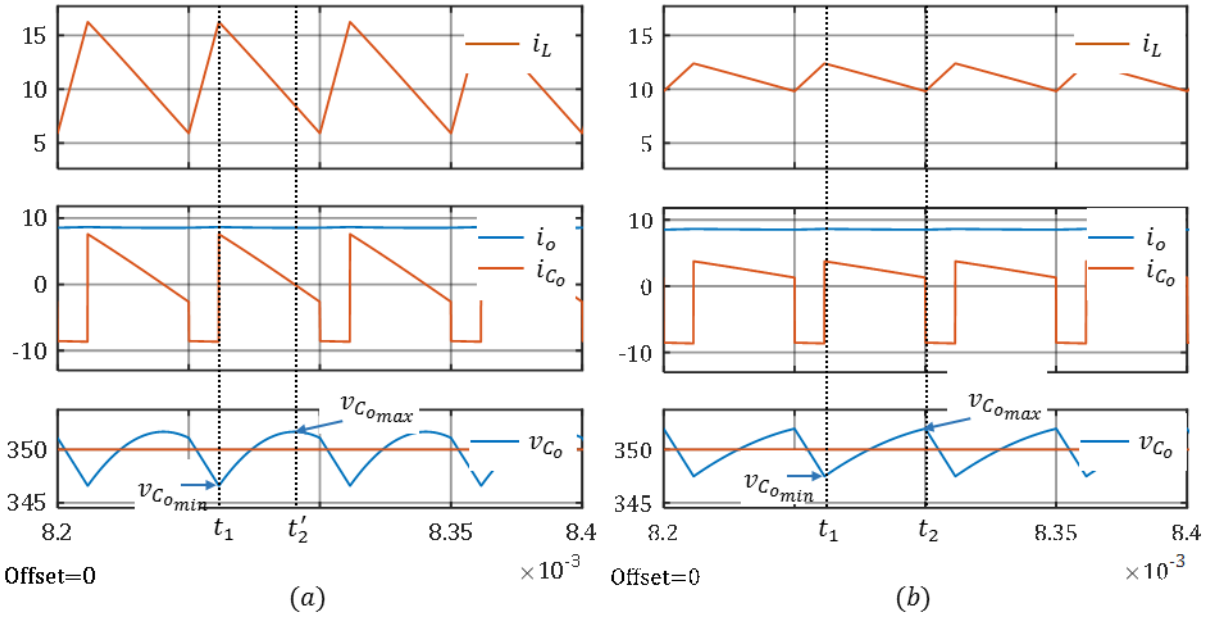


Fig. 3.17 Steady state i_L and v_{C_o} waveforms ($L = 300\mu H (a), L = 1.2mH (b), C_o = 22\mu F, f_s = 20kHz, V_o = 350V, P_o = 3kW, V_{in} = 270V$).

According to the last expression, as expected, a higher switching frequency represents a benefit in the choice of the capacitance value. The inductance value L may affect the C_o value through the current ripple value Δi_L, this influence only appears for $L < L_{lim}$. This comes as no surprise for the boost converter since the amount of charge absorbed by the capacitor C_o mostly depends on the DC value of i_L and the load power, rather than from the current ripple.

3.4.2.1 Capacitor parasitic effects

The discussion and the analytical condition obtained so far are true if the capacitor is considered as an ideal capacitance. In practice, the real impedance of the capacitor results more complex. At high frequencies, the board layout, the connection wires and magnetic coupling phenomena affect the impedance profile of the component. Around the switching frequency, a reliable lumped parameters model of the capacitor consists of a capacitance, a series resistance and a stray inductance. The interaction of these parasitic components, especially the stray inductances, with the discontinuous current conducted by the capacitor, may lead to dangerous voltage surges. The manufacturers usually provide these parameters and the capacitor impedance profile as function of the frequency (Fig. 3.18), but the layout of the board and the patristic effects of the conductor traces must be accounted.

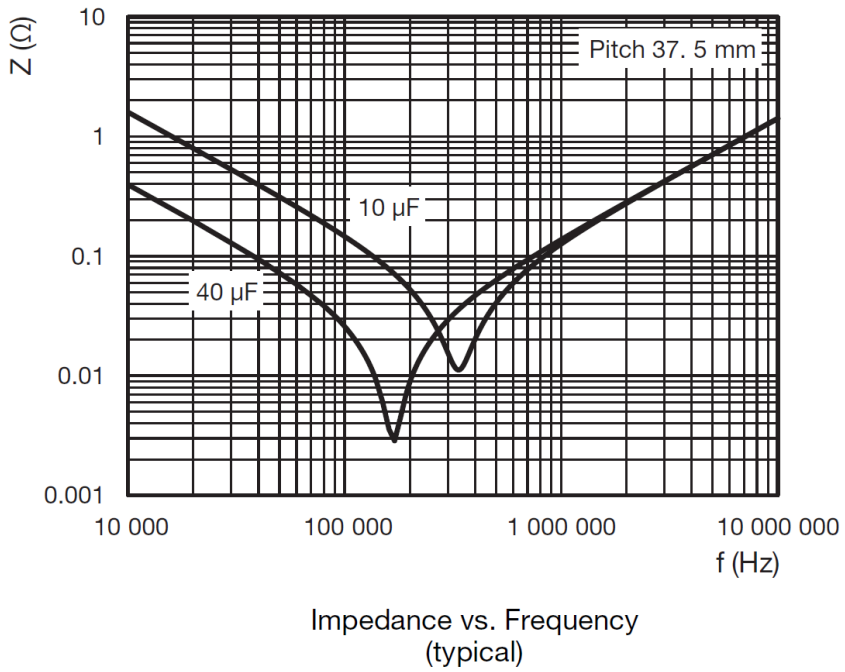


Fig. 3.18 Capacitor impedance as function of the frequency [115].

Fig. 3.18 shows how the resonance frequency of the capacitor decreases along with the capacitance value. In order to minimize these effects, beyond a proper layout of the board, a bank of capacitors is often used, composed of a multiplicity of smaller capacitors connected in parallel instead of a bulky one [117], especially when dealing with WBG semiconductor devices. Concerning the capacitor technology, polypropylene film capacitors are often preferred because of their low loss characteristics at high frequencies.

3.4.3 EMI Filter

In order to protect the main network from current harmonics, all the converters should include an input EMI filter. Indeed, the reliability and the normal operation of the devices connected on the grid could be disturbed or even damaged by the current and voltage noise emitted on the DC bus, or conversely, the load converter normal functioning and safety could be compromised by the disturbances coming from the network. Usually, to prevent these circumstances, each application is regulated by a standard normative. This standards impose a set of requirements and experimental tests towards the radiated and conducted emissions and susceptibility of each converter interfaced on the grid.

In this work, only conducted emission of the converter under study are considered. Indeed, a convenient approach to contain the radiated emissions, is to limit their sources, then the conducted ones. Anyway, the modelling and the validation of the radiated emission compatibility require a specific study and expensive instruments, which were not available at the laboratory.

The emission requirements involve a wide range of frequency. For example, the DO-160F standards, which includes a list of environmental conditions and test procedures for airborne equipment redacted by RTCA Inc., cover a range of frequencies of emitted noise from very low values (AC modulating signals around 300 Hz) up to 152MHz. Namely, two range of frequencies can be considered for the conducted case:

- Low frequencies requirements ($f < 150\,kHz$), mostly applied in the audio range of frequencies, include harmonic distortion and current modulation tests for the AC equipment and current ripple requirements for the DC equipment.

- High frequency requirements are employed in the radio spectrum, from 150 kHz up to 152 MHz, for all the electrical equipment.

3.4.3.1 Low frequency rejection

The normal operation of a SMPS leads to the generation of high frequency harmonics because of the switching elements. In a DC/DC converter, the differential input filter purpose is to suppress the differential noise at the input terminal at the switching frequency. The DO-160F standards define the low frequency constraints for the only differential conducted mode, for frequency values up to 150 kHz. In the specific case, a DC/DC converter with input voltage of 270V and operating power in the range [1kW, 10kW] belongs to the D category of the aforementioned standards DO-160F, which state that the peak-peak value of the individual equipment's line current ripple shall not exceed 0.140 times of the individual equipment's maximum DC current drawn.

In our study, the harmonics multiple frequencies of f_s were supposed to require a minor attenuation than the fundamental one at f_s. Then, the differential input filter is designed to reduce the first harmonic of the boost inductance current, in order to keep the input current ripple within the required constraints ($\Delta i_{L_{fil}} < \Delta i_{lim}$).

The input current of a boost converter has a periodic asymmetrical saw-tooth shape. The first harmonic coefficient $b^{(I)}$ of the Fourier series expansion can be expressed as:

$$b^{(I)} = \frac{1}{D(1-D)\pi^2}\ sin\big((1-D)\pi\big) \tag{3.74}$$

The resonance angular frequency ω_{res} and the order of the filter has to respect the following condition:

$$Att_{DM}(f_s) = \frac{\Delta i_{lim}}{b^{(I)}\Delta i_L} \cong \left|\frac{\omega_{f_s}^2}{\omega_{fil}^2} - 1\right|^{-l} \tag{3.75}$$

In (3.75), $\omega_{f_s} = 2\,\pi\,f_s$ is the angular switching frequency, $b^{(I)}$ is the Fourier first harmonic amplitude of the boost inductor current i_L and l is the number of LC stages, which defines the order of the filter. The input filter capacitance C_{fil}, along with L_{fil} inductance, defines the value of the cut-off frequency ω_{fil} and the attenuation of the filter:

$$\omega_{fil} = \big(C_{fil}\,L_{fil}\big)^{-\frac{1}{2}} \tag{3.76}$$

To increase the attenuation of the filter, a smaller cut-off frequency, hence a bulkier filter is needed (greater values of C_{fil} and L_{fil}).

The attenuation depends on the amplitude of the i_L current first harmonic, hence the Δi_L ripple amplitude from (3.75). It is clear that the choice of the filter components is directly affected by the values of L and f_s. The trade-off between the choice of the L inductor, the switching frequency f_s and the filter components is needed to optimize the overall size of the converter. The L_{fil} and C_{fil} values influence not only the size of system, but also the stability of the system. Indeed, the interaction of an LC filter with the input impedance of the converter may lead to instabilities, especially if the resonance frequency of the filter lies within the gain-bandwidth of the controlled system. That means filters with low value of resonance frequency (high attenuation required, then high values of L_{fil} and C_{fil}) are more likely to impair the stability of the system. This issue is further discussed in Chapter 4.

3.4.3.2 High Frequency rejection

The high frequency behaviour of a switched mode power supply is a far more complex issue. At these frequencies (in the MHz range), it depends indeed on many parameters, such as converter topology, power ratings, components parasitic elements, and board layout. The conventional design procedure of the input filter consists into a measure routine of the conducted emission of the device under test by using a line impedance stabilization network (LISN) (Fig. 3.21) and a network analyser. Those monitoring should be performed according to standardized procedures which ensure the repeatability of the results. The common and differential current noises are evaluated as:

$$i_{CM} = \frac{1}{2}\frac{v_1 + v_2}{50\Omega}, \qquad i_{DM} = \frac{1}{2}\frac{v_1 - v_2}{50\Omega} \tag{3.77}$$

where v_1 and v_2 are the voltages measured by the spectrum analyser (with impedance at the input terminals set to 50Ω) referred to Fig. 3.21.

The high frequency noise can be distinguished into differential mode (DM) and common mode (CM) noise. The DM noise involves the undesired current and voltage disturbances measured between the positive and negative input terminals of the device under test. The common mode noise consists of the disturbances between the hot input terminals and the ground potential of the device. Indeed, at high frequencies, the parasitic capacitances between the circuit nodes and the ground of the system provide a path for the current if the node exhibits fast variations of its potential. Two different filters are designed to prevent those interferences.

A lumped parameter model of the circuit has been simulated in SABER environment, as shown in Fig. 3.19. The circuit model takes into account all the stray inductances and the parasitic capacitances toward the ground potential. The lumped parameters have been tuned in order to reproduce the S_1 experimental transient waveforms v_{DS} and i_{DS}. A high frequency model of the SiC MOSFET devices has been modelled through the Architect Model tool available in SABER (Fig. 3.20).

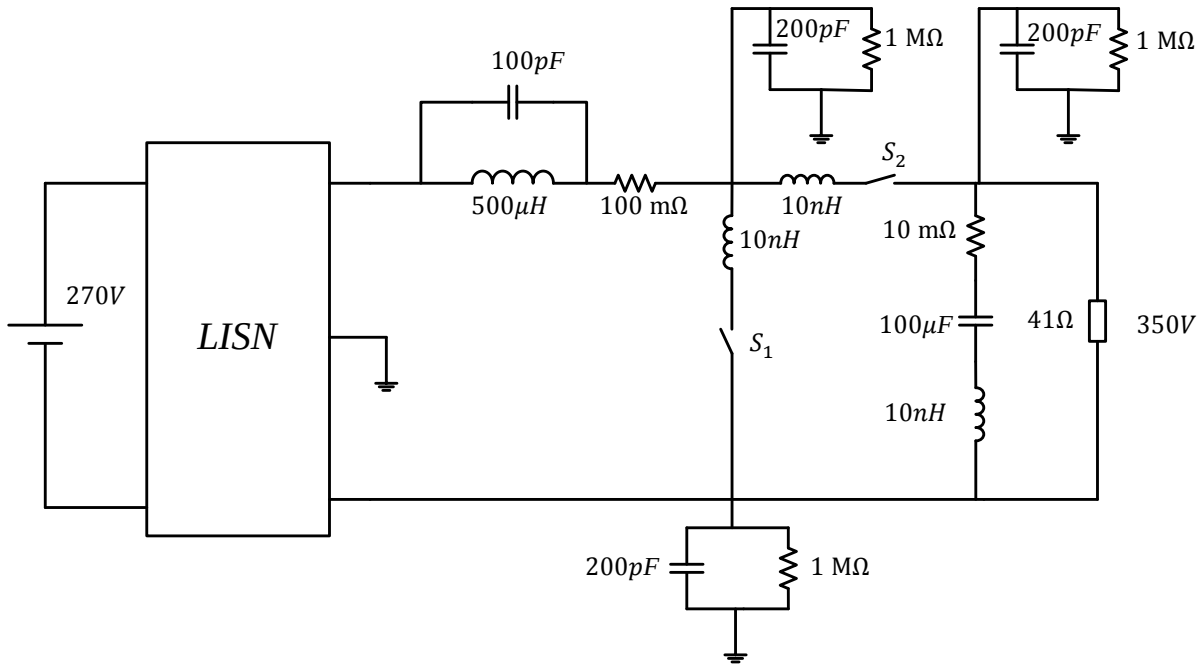


Fig. 3.19 High frequency Boost lumped parameter model ($V_{in} = 270V, V_o = 350V, f_s = 30kHz,\ L = 500\ \mu H, C_o = 100\mu F, P_o = 3kW$).

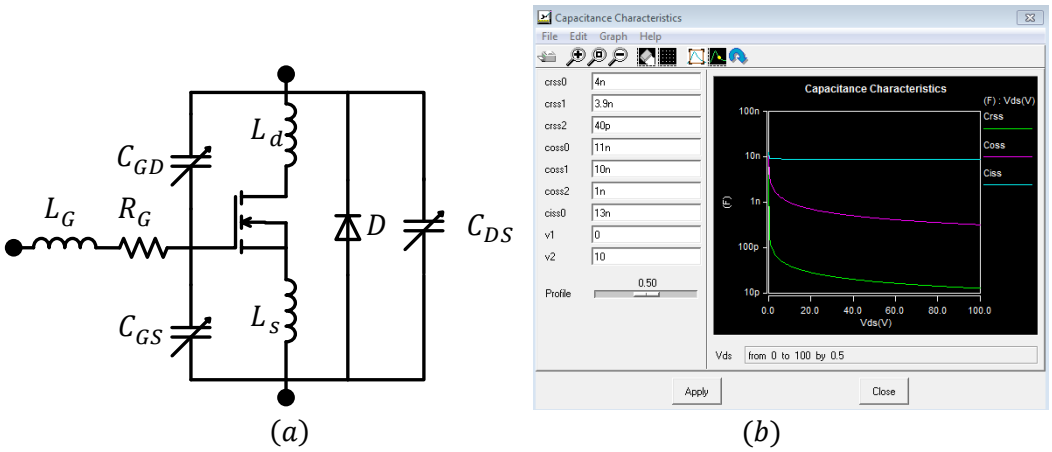


Fig. 3.20 Architect model tool available on SABER environment.

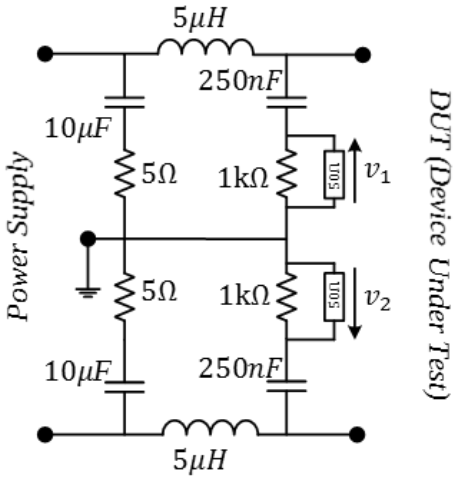


Fig. 3.21 LISN as defined in DO-160F.

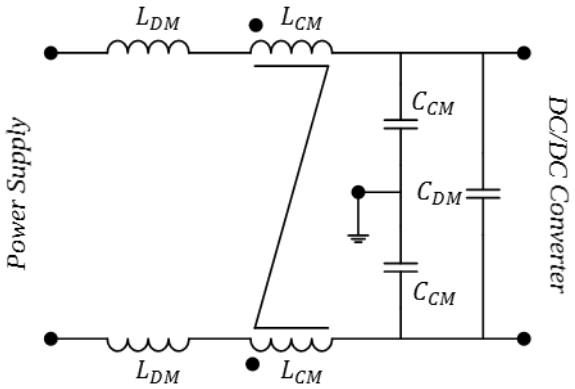


Fig. 3.22 Second order input filter example for the rejection of both the differential and common modes.

The simulated CM and DM spectrum are compared with the maximum admitted radiofrequency interference boundaries in Fig. 3.23. For each mode, the required cut-off frequencies of the DM and CM second order filters (shown in Fig. 3.22) are chosen in order to attenuate the noise amount which exceed the limits, as shown in Fig. 3.24.

The specified boundaries have to be increased by a security leeway of 3dB, in order to prevent the eventual sum of the two modes.

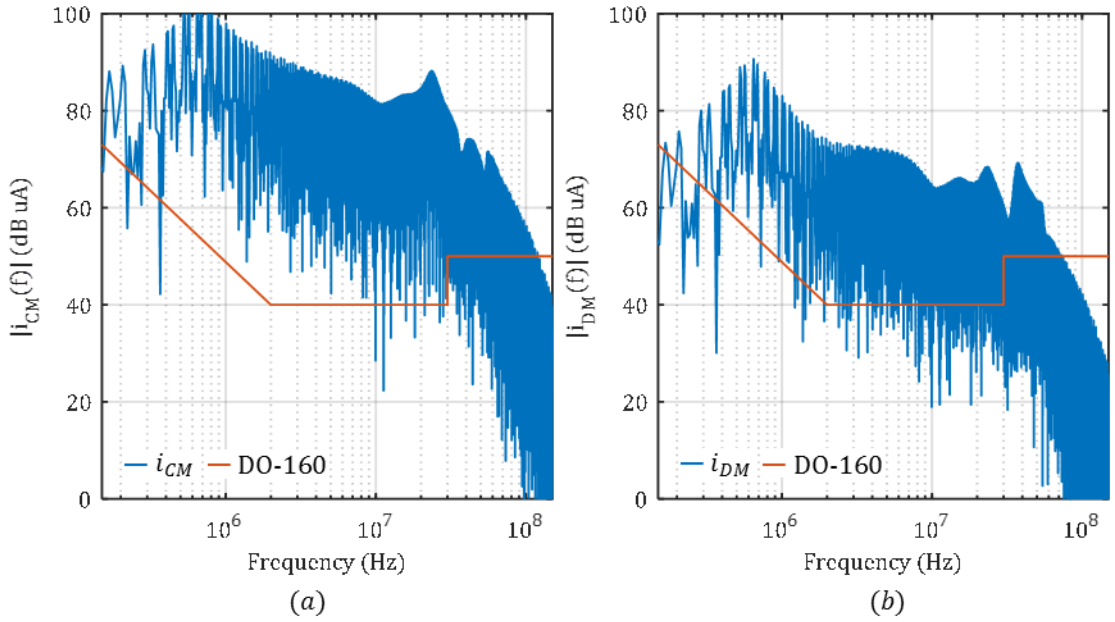


Fig. 3.23 FFT spectrum of the i_{CM} (a) and i_{DM} (b) currents based on SABER simulations compared with the high frequency DO-160.

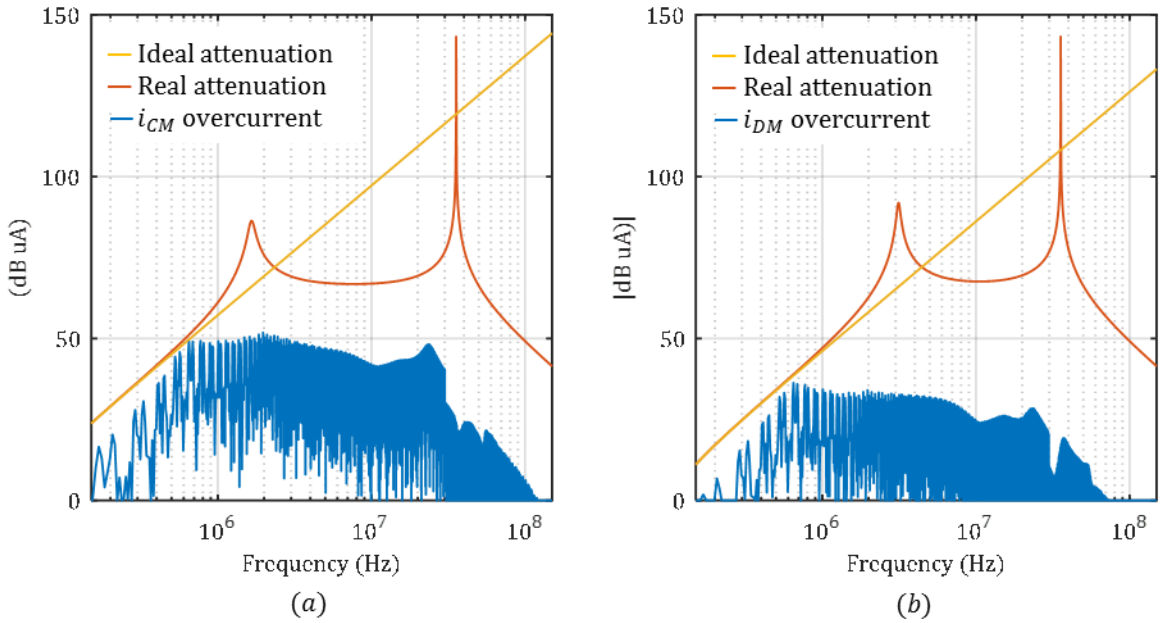


Fig. 3.24 Ideal and real CM (a) and DM (b) overcurrent noise rejection by a second order LC filter ($\omega_{fil}^{(CM)} = 2.51 \cdot 10^5 rad/s$, $\omega_{fil}^{(DM)} = 4.4 \cdot 10^5 rad/s$).

An input filter shall be designed in order to provide the required attenuation. In Fig. 3.24, a DM and CM input filter as the one showed in Fig. 3.22 has been designed to suppress the exceeding common mode and differential mode noises. Nevertheless, the real filter attenuation resents of the not ideal frequency behaviour of the filter components. Fig. 3.24 also depicts the more realistic attenuation profile, which takes into account the parasitic capacitance of the filter inductance, the inductance permeability decay due to the frequency dependence, the parasitic inductances and resistances due to the connections.

In fact, the input filter for high frequency conducted noise rejection should be tested on the test bench to verify that the deleterious effect of the non-ideality of the filter components on the attenuation does not compromise the compliance with the standard constraint of the application.

The knowledge of the high-frequency behaviour of the power circuit and the input filter deserves an intensive study and modelling work through the use of instruments such as spectrum analysers, impedance analysers or numerical finite element analysis tools. The building of such high-frequency models requires experimentation that goes beyond the objectives of this work. For this reason, the design of the filter for the rejection of high-frequency noise was not included in the optimization procedure illustrated in the manuscript.

3.5 Conclusions

Chapter 2 focused on the advantages of the employ of a DC/DC converter for a powertrain embedded application in the frame of MEA or EV/HEV.

However, in order to derive maximum benefit from the inclusion of the DC/DC converter in the conversion chain, compactness and efficiency require an appropriate design. In this chapter, the main elements of a converter have been discussed and their role and impact in the converter performances were analysed.

The switching devices deserved a particular attention, since its non-linear behaviour requires a precise model to understand and analytically evaluate the conduction and switching performances, namely the commutation times and the power losses. Power losses and switching times of the switching device represent indeed the main limiting factors for the switching frequency. Particularly, the analysis of the dynamic behaviour demonstrates the main advantages brought by fast switching devices, like the WBG based ones.

The converter power device is probably the most influent component on the converter performances and on the consequent design choices. Indeed, the WBG devices innovation brought an intensive development of the power electronics systems in terms of efficiency and compactness. Usually, the most of the power losses in a SMPS are wasted by the semiconductor devices.

Concerning the conduction power losses of the devices, they depend on the selected switching device and by the operating point parameters (duty cycle, nominal current). On the other hand, more parameters affect the switching power losses. The charging profile of the device is related to the driving circuit parameters (in the considered case only the gate resistance has been considered). Depending on the charging profile of the device, then on the commutation times, the operating switching frequency f_s of the converter shall be chosen. Indeed, the selected switching device technology, material and ratings determine the maximum switching frequency that can be achieved to operate within the device safe operating temperature.

The switching frequency affects the power losses and particularly the size and the weight of the converter in several ways. As mentioned, the amount of switching losses determines the size of the heatsink of the converter. Furthermore, as shown in Chapter I, the harmonic content at high frequencies brought in the circuit increases along with the switching frequency. The EMI input filter for the high frequency rejection ($f > 150kHz$) is then designed to provide a higher attenuation of the common and differential conducted noise to comply with the application standards requirements. Furthermore, it shall be pointed that the gate resistance, along with the intrinsic capacitances of the device, has a strong impact on the switching times of the device, hence on the current/voltage slopes of the switches. High dv/dt and di/dt lead to a greater harmonic content at high frequencies, hence it leads to the choice of a bulkier EMI filter. Of course, shorter switching times improve the power losses and the cooling system size.

On the other hand, a high switching frequency will benefit the passive devices. Basically, a faster magnetic/static energy balancing among the passive components reduces the stored energy, which helps

reducing their size. The classical design approach of the passive components has been discussed, with a particular emphasis on the interdependencies between the parameters' selection. The design of the magnetic components, for example, involves several possibilities concerning the size, the material and the coils number, even for a given value of inductance. It was highlighted the mutual influence between switching frequency and the values of capacitances and inductances of the converter and the input filter, besides their impact on the size of the passive components and on the cooling system.

Furthermore, the design of the converter's power stage impacts in the design of the control strategy.,Indeed, for the dynamic model of the converter to be valid, the bandwidth of the controller, hence of the closed loop system, cannot be chosen too close to the switching frequency. In case of variation of the operating point, if the controller bandwidth is limited, the passive components should sustain the current/voltage variations and keep them within reasonable values, hence they should be designed accordingly. Those considerations will be thoroughly developed in the following chapter.

The components' design parameters and the performances models presented so far will be valuable for Chapter 5 to perform a global optimization of the converter.

4 Dynamical Analysis and Control Strategy of a DC-DC converter

4.1 Introduction

So far, the design considerations were made for the only steady state behaviour of the converter. If the operating point is likely to change during the course of the mission cycle, the dynamic behaviour of the closed loop system converter-controller becomes of primary importance in the design process, as well as the size or the efficiency of the converter.

In a DC embedded network, such as the HEV and the modern aircraft ones, the active loads can possibly increase or lower their demand of power more or less abruptly, depending on the load [118], [119]. The converters shall be designed to correctly supply these loads, even dealing with fast current and power transitions. In case of a large variation of the active load powers connected to the DC/DC converters output, these converters may exhibit large excursion of the output voltage in transitory states. When these dynamic voltage variations disturb the control of the active loads, the passive components of the converter and its controller have to be designed accordingly to keep the voltage variation within an acceptable range.

In the case of a motor driver application, the benefits provided by a joint employ of a DC/DC converter and a DC/AC inverter have already been discussed in Chapter 2. The motor driving conversion chain is showed in Fig. 4.1 for the specific case of a permanent magnet synchronous motor, with the inverter control scheme [120] (Fig. 4.1(b)).

During a strong increase of the motor torque required (then of the current references $i_{d_{ref}}$ and $i_{q_{ref}}$ in Fig. 4.1), a large variation of the DC/DC converter load power occurs, because of the rapidity of the inverter phase currents controller. Under these conditions, if the inverter input voltage v_{DC} (the DC/DC converter output voltage) exhibits an important undershoot, the controllability of the motor phase currents is compromised (as mentioned in Chapter 2). The inner current regulator (Fig. 4.1(b)) of the inverter controls the inverter currents in the $dq0$ domain, and provides a voltage reference v_{ref} in the abc coordinates for a PWM (or in the Clarke coordinates for a space vector modulator), for the generation of the command signals of the inverter switches. Fig. 4.2 shows the decision space of the modulator, in $dq0$ coordinates. The magnitude of the reference vector v_{ref} should lie within the circle with radius of ½ v_{DC}, for a sine generated PWM, of $1/\sqrt{3}\ v_{DC}$ for a space vector modulator.

If the reference v_{ref} exceeds the above mentioned values, the modulator block enters in an over-modulation state, where the controllability of the motor is no longer ensured. The DC/DC converter in Fig. 4.1(a) needs then to be designed in order to avoid excessive undershoot of its output voltage and keep it within a specified range.

In the following chapter, the design of the control network of a DC/DC converter will be discussed. As briefly introduced, the analysis of the dynamic behaviour of the converter will be developed mostly for the small signals, hence in the linear domain. This allows to employ linear tools for the characterization in the frequency domain of the system transfer functions, like Bode or Nyquist diagrams.

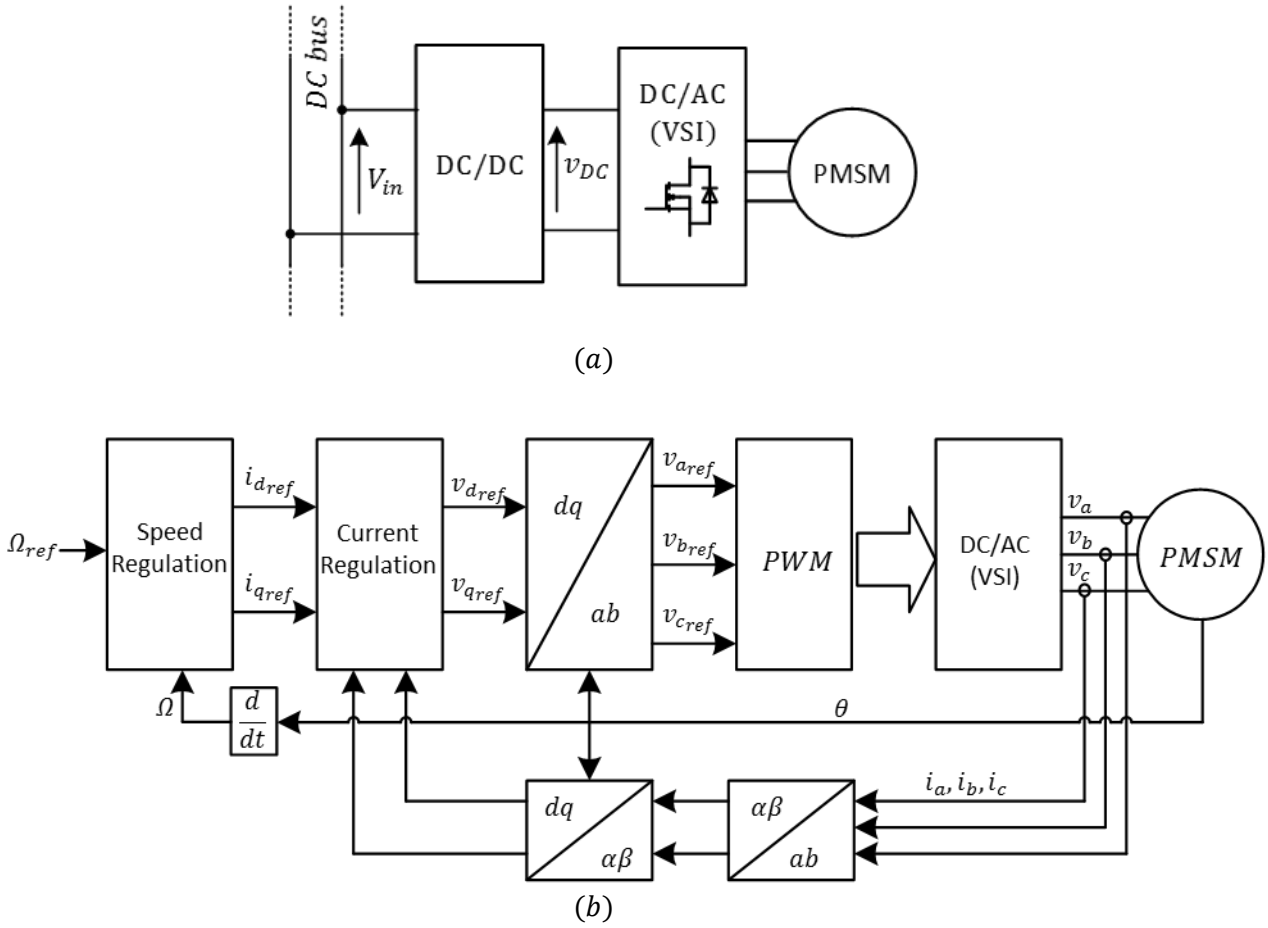


Fig. 4.1 Motor drive electrical scheme (a) and example of field oriented control scheme of the PMSM (b).

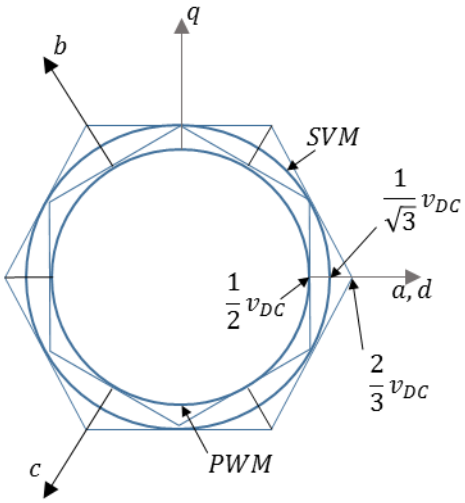


Fig. 4.2 Decision space of a pulse width modulator and a space vector modulator.

From the conducted analysis, it will be clear that a double loop control strategy is desirable. Indeed, the single loop strategy, mostly preferable for low power applications, presents several problems linked to the stability of the system, due to the presence of the right half plane zero, a common issue in the boost derived converters. The double loop control strategy allows to overcome this issue and to control the inductor current as well, then improve the reliability of the system in case of disturbances or variations of the operating point.

The chosen current regulator consists of a peak current controller, a robust and largely employed method. For the considered application, one of the main tasks is to ensure the low excursion of the output voltage in case of load transient variations, as for example during a variation of the mechanical load. For this reason, an energy regulator has been preferred for the control of the output voltage [121], especially because of its ability to reject output power disturbances.

Once the control strategy has been chosen, an analytical method has been proposed to design the output capacitor of the converter in order to respect the voltage constraints on the output terminals in case of a variation of the output load power. Such method takes into account the controller parameters as well, since the transient behaviour of currents/voltages through the passive components during disturbances or variations of the operating point strictly depends on the controller features (bandwidth, duty cycle saturation etc.).

In view of the thesis main objective, which consists in a global optimization of the DC/DC converter, the proposed approach allows to design the converter passive components by taking into accounts the transient behaviour and the controller parameters as well.

Furthermore, as showed in Chapter 3, in order to keep the harmonic content on the DC bus below the standards' limitations, the DC/DC converter shall be connected through an input filter. On the other hand, the differential input filter may interact with the power stage and provoke instability issues, especially when it comes to deal with a constant power load (CPL).

When the load is an actuator as shown in Fig. 4.1, the current loop of the DC/DC converter is designed with high dynamical properties. That implies the power supplied to remain practically unchanged. For this reason the actuator can be considered as a constant power load. The instability issues derived from the interaction of the input filter and the negative impedance of a CPL are discussed, along with the most suitable approaches to verify the stability of the closed loop system. Indeed, due to the frequency limitations of the linear models, in order to verify the stability of the system in a wider range of frequencies (even close to the switching one), a discrete modelling approach is shown and employed [122], [123].

4.2 Dynamical model of a DC/DC switched converter

For purposes concerning the control and the stability analysis of the closed loop system, the system shall be represented with a dynamical model. Within the switching period T_s is steady state, a SMPS (switched-mode power supply) is characterized by N possible configurations. Each i^{th} configuration of the converter can be described by an ordinary differential equations system represented by the i^{th} function f_i:

$$\dot{\boldsymbol{x}}(t) = \boldsymbol{f}\big(\boldsymbol{x}(t)\big), \boldsymbol{x} \in \mathcal{R}^n, \boldsymbol{f}: \mathcal{R}^n \to \mathcal{R}^n, t \in T_i \tag{4.1}$$

Where $\boldsymbol{x}$ represent the state variable vector, n is the order of the system, T_i is the time interval of the i^{th} configuration and $\boldsymbol{f}$ is the vector function which defines the relationship between the state variables and their time derivative. The relationship in (1.7) can be considered linear and time-invariant within each i^{th} sequence in the period T_i, since the active devices, which are the only non-linear elements in the circuit, are supposed as a short circuit (a resistance or/and a voltage drop for average switch models [33], [93]) in on-state, or an open circuit in off-state. Nevertheless, the converter shall be designed for dynamical variations of the operating point, such as disturbances or variation of the controller loop reference, which have far larger transition times than the converter switching period T_s, hence the configurations periods T_i.

In order to observe the low frequency dynamical behaviour of the system, several approaches are employed in literature [33], [62], [93]. A first approach consists into averaging the state variables over

one switching period, so to cut out the switching frequency ripple of the passive components. A slightly different approach consists in the *state-space averaging* method, in which the system is firstly represented through the state space representation (matrix form) and consequently averaged over a switching period. A third method is the *average switch model*, in which the current and voltage waveforms of the only switching devices are averaged and replaced by an equivalent quadrupole. The three approaches are consistent and provide the same results. The large signal average models, nevertheless, in most part of the cases do not provide linear equations between the state variables and the control inputs $\boldsymbol{u}(t)$ (duty cycles):

$$\dot{\boldsymbol{x}}_{av}(t) = \boldsymbol{f}_{av}(\boldsymbol{x}_{av}(t), \boldsymbol{u}(t)) \tag{4.2}$$

In order to study the converter in the frequency domain through techniques of conventional circuit analysis, the system should be linearized around the operating point. To construct a small signal AC model, the variables and the control input of the system are decomposed in a mean value (at the operating point) and an AC small signal perturbation value. Such linearization can be equivalently obtained by developing the Taylor expansion of the system and retaining only the linear terms.

Due to the linearization step, such model is reliable just within a limited neighbourhood of the operating point. Furthermore, due to the averaging of the state variables over the switching period, its accuracy cannot be ensured for frequency values close to the switching one (usually it is employed up to a limit frequency one or two decades lower than the switching one), hence the need of a different model approach.

A modelling approach that provides a more reliable dynamic description of the system consists in the discrete-time modelling approach [124], [125]. The cyclic behaviour of the system in steady-state is represented by a discrete time map of the state space vector (Poincaré mapping method) with a sampling period equal to the switching one (T_s):

$$\boldsymbol{x}[(n+1)T_s\,] \;\; = \boldsymbol{f}[\boldsymbol{x}(n\,T_s\,), \boldsymbol{u}(n\,T_s)] \tag{4.3}$$

The term $\boldsymbol{x}(n)$ in (4.3) is the state variables vector at the beginning of the n^{th} switching period. The vector function $\boldsymbol{f}$ is the analytic expression which relates the state vector at the time $(n+1)T_s$ and the one at the time $n\,T_s$, obtained by analysing all the operating sequences of the converter. Such model, even if relatively harder to deduct, is particularly suitable to analyse chaotic behaviour, bifurcation phenomena because of its accuracy at frequency values close to the switching one. In this thesis work, it is employed to analyse the stability issues due to the interaction between the output impedance of the input filter and the input impedance of the converter, when the resonance frequency of the filter is too close (less than two decades) to the switching frequency.

4.3 Boost dynamical behaviour

4.3.1 Frequency domain stability analysis

In this section, the stability and the control analysis of the equivalent time-invariant model of the converter is verified and discussed in the frequency domain, namely in the *s*-plane. Laplace transform is used to easily map the time domain differential function in the frequency domain. From the obtained system in the Laplace frequency variable *s* it is possible to deduce the Laplace transfer functions relative to the system state variables. In terms of stability, usually, a particular attention is paid to the control-to-output and the open loop transfer functions [33], [93]. One of the most employed methods for the stability analysis of linear system is surely the Nyquist stability criterion [126], [127]. The criterion is

based on two concepts from complex variable theory, *contour mapping* and the *Principle of the Argument* [128], [129], and it provides a necessary and sufficient condition for closed-loop stability based on the open-loop transfer function. For the specific case of SMPS small signal models, where usually the open-loop transfer functions are stable and do not present any right half plane singularities, the Bode stability criterion is mostly applied. Two stability indicators are provided by the Bode plot, namely gain margin g_m and phase margin φ_m as showed in Fig. 4.3 for a generic transfer function $L(s)$ ($s = i\,\omega$).

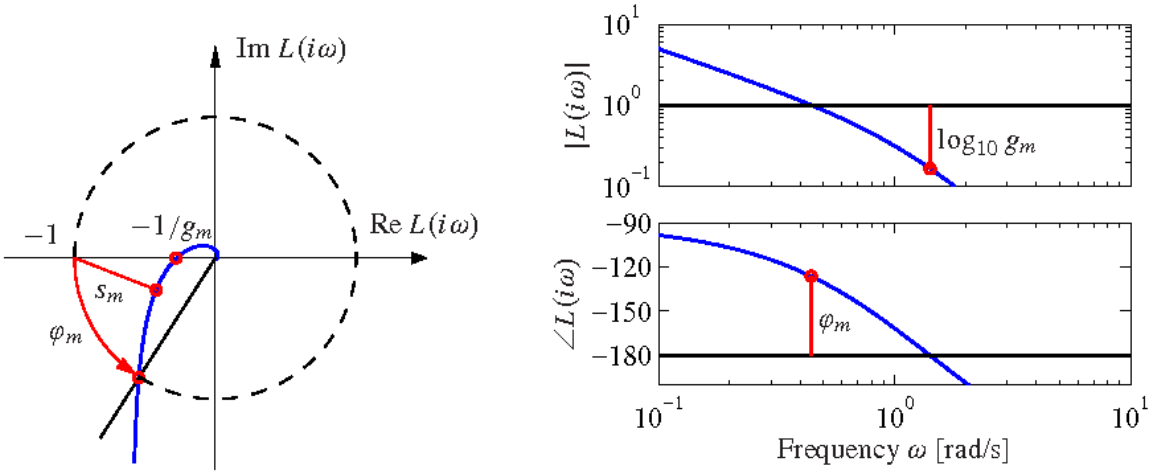


Fig. 4.3 L(s) ($s = i\omega$) transfer function mapping in the polar coordinates plot (a) and Bode plot (b).

These quantities, along with the crossover frequency ω_c of the open-loop transfer function, provide an important information about the performance and the robustness of the controlled system. Indeed, the cross-over frequency ω_c defines the bandwidth of the controlled system, in terms of reference tracking. The phase margin φ_m indicates how much the feedback signal can be delayed at the crossover harmonic, before any instability occurs. Similarly, the gain margin g_m represents how much the signal should be amplified at the frequency where the phase is -180° before the system becomes unstable.

4.3.2 Boost dynamical analysis

The large signals average model for a simple DC/DC boost converter in continuous mode (Fig. 4.4) is described as:

$$\begin{cases} L\dfrac{di_L}{dt} = V_{in} - (1-d)\,v_{C_o} \\ C_o\dfrac{dv_{C_o}}{dt} = (1-d)i_L - \dfrac{v_{C_o}}{R} - i_o \end{cases} \tag{4.4}$$

For ease of discussion, the model does not include any resistances neither voltage drops of the switches. The load consists of a resistance R and a current source i_o which models possible disturbances of the load power. The value d represents the duty cycle of the command signal $u = u_1$ of the switch S_1 in Fig. 4.4. The average model is clearly not linear (product between input and state variables), and it needs to be linearized around the nominal operating point. The AC small signal model is evaluated for an operating point defined by an input voltage V_{in} and a fixed average output voltage V_o. The steady state average values of the input and state variables are evaluated as:

$$\begin{cases} < v_{C_o} >_{T_s} = V_o \\ < i_L >_{T_s} = I_L = \dfrac{V_o^2}{R\, V_{in}} \\ < d >_{T_s} = D = 1 - \dfrac{V_{in}}{V_o} \end{cases} \tag{4.5}$$

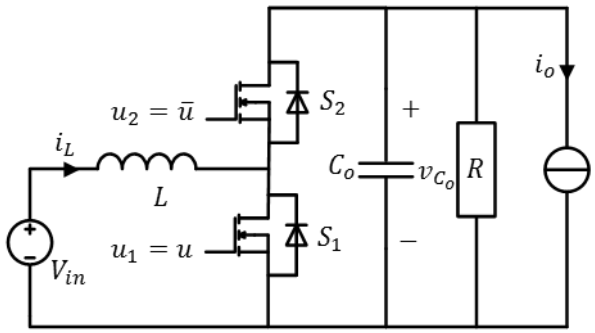


Fig. 4.4 DC/DC Boost converter.

For the described operating point, the converter is assumed lossless. The AC small signal system describes the dynamic behaviour in the neighbourhood of the operating point defined in (4.5). The linear model of the converter is expressed as:

$$\begin{cases} L\dfrac{d\tilde{\imath}_L}{dt} = \tilde{v}_{in} - (1-D)\tilde{v}_{C_o}(t) + \tilde{d}\, V_o \\ C_o\dfrac{d\tilde{v}_{C_o}(t)}{dt} = (1-D)\tilde{\imath}_L(t) - \tilde{d}\, I_L - \dfrac{\tilde{v}_{C_o}(t)}{R} - \tilde{\imath}_o \end{cases} \tag{4.6}$$

Where $\tilde{x}$ indicates the small signal perturbation of the state/ input variables and the uppercase symbols refer to the variables mean value at the operating point. The quantities $\tilde{\imath}_o$ and $\tilde{v}_{in}$ represent the perturbations on the output load and on the input voltage V_{in}, respectively. Now that the system represented in (4.6) is linear and time-invariant, it can be mapped in the frequency domain through the Laplace transform:

$$\begin{cases} s\, L\, i_L(s) = v_{in}(s) - (1-D)v_{C_o}(s) + d(s)\, V_o \\ s\, C_o v_{C_o}(s) = (1-D)i_L - I_L\, d(s) - \dfrac{v_{C_o}(s)}{R} - i_o(s) \end{cases} \tag{4.7}$$

The dynamic response of the converter to the input signal variation is described by the small signal transfer functions, which relate the state variables and the input variable or the disturbances in the frequency spectrum. The output voltage v_{C_o} is the controlled variable in the considered case, then it is of primary importance to analyse its variation in response to the input variable perturbation in order to design a proper controller:

$$G_{vd}(s) = \left.\frac{v_{C_o}(s)}{d(s)}\right|_{\substack{v_{in}=0, i_o=0 \\ open-loop}} = \frac{V_{in}}{(1-D)^2}\frac{\left(1-\dfrac{s}{\omega_{RHP}}\right)}{1 + s\dfrac{2\zeta}{\omega_0} + \dfrac{s^2}{\omega_0^2}} \tag{4.8}$$

Where

$$\omega_{RHP} = \frac{R(1-D)^2}{L} \tag{4.9}$$

$$\omega_0 = \sqrt{\frac{(1-D)^2}{LC_o}} \tag{4.10}$$

$$\zeta = \frac{1}{2R(1-D)}\sqrt{\frac{L}{C_o}} \tag{4.11}$$

The control-to-output transfer function $G_{vd}(s)$ in (4.8) is found by solving the equivalent small signal model in (4.7) for $v_{C_o}(s)$, where the Pulse Width Modulation (PWM) block gain has been assumed unitary.

In Fig. 4.5, the Bode representation of the G_{vd} transfer function is showed for $L = 200\mu H$, $C_o = 100\ \mu F$, $V_o = 350V$, $V_{in} = 270V$ and for increasing values of the load resistance R.

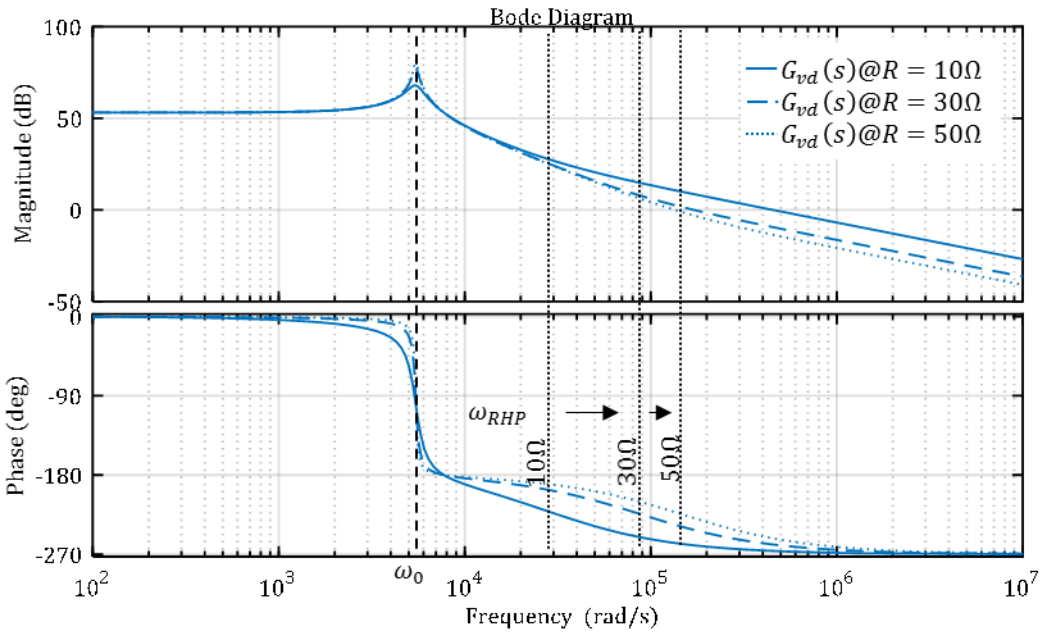


Fig. 4.5 Bode plot of the G_{vd} control-to-output transfer function of the Boost converter ($L = 200\mu H$, $C_o = 100\ \mu F$, $V_o = 350V$, $V_{in} = 270V$ and $R = 10\Omega, 30\Omega, 50\Omega$).

The usual bode plot relative to a switching converter control-to-output transfer function is similar to a low pass filter, where the resonance frequency, the bandwidth and the number of resonances depend on the passive elements values and the operating point. In the case of a simple chopper converter, it behaves as a second order low pass filter with two complex and conjugated poles with magnitude ω_0.

As shown in Fig. 4.5, the variation of the load resistance R affects the damping of the system, hence the peak of the G_{vd} resonance in ω_0. In Fig. 4.5, the value ω_{RHP} represents the value pulsation of the right-half plane zero (RHPZ), which has a deleterious effect on the G_{vd} phase profile common in all the boost derived converter topologies, as it will be further discussed below. A higher value of the load resistance R, i.e. a lower value of the supplied power, provokes a shift of the RHPZ toward higher frequencies.

It is worth remarking that no resistive elements have been accounted until now. The DCR_L series resistance of the L inductor contributes to dump the transfer function resonance in ω_0, by increasing the damping factor ζ in (4.11). The ESR series resistance of the output capacitor C_o, in particular, contributes with a left-plane zero at high frequencies [93]:

$$\omega_{ESR} = -\frac{1}{ESR_{C_o}\, C_o} \tag{4.12}$$

This zero could be beneficial, since it increases the phase. Nevertheless, especially with a capacitor bank composed of several capacitors in parallel, the equivalent value of the ESR is very low, hence the phase increase usually occurs at frequencies far higher than ω_0 and ω_{RHP} to actually benefit from it.

A first control approach consists in a single loop regulator which controls the output voltage, as shown in Fig. 4.6:

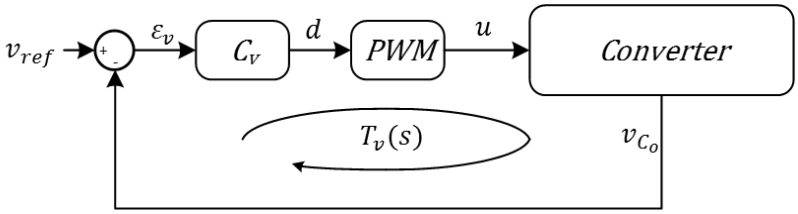


Fig. 4.6 Single loop voltage mode control scheme.

A linear PI controller should ensure the rejection of DC error and the necessary phase boost to ensure a satisfying phase margin at the desired frequency ω_c, which represents the bandwidth of the closed-loop system, or else the crossover frequency of the open loop system $T_v(s)$:

$$\omega_c = \{\omega \in \mathbb{R} \mid |T_v(i\omega_c)| = 1\} \tag{4.13}$$

$$T_v(s) = \left.\frac{v_{C_o}(s)}{\varepsilon_v(s)}\right|_{v_{in}=0, i_o=0} = C_v(s)\, G_{vd}(s) \tag{4.14}$$

with $C_v(s)$ as the Laplace function of the PI voltage controller and $\varepsilon_v = v_{ref} - v_{C_o}$. The controller bandwidth ω_c must be chosen at pulsations far away from the resonance pulsation ω_0, in order to avoid dangerous interaction with the abrupt phase falling and the resonance of the magnitude of G_{vd}. For example, in the case of the $T_v(s)$ function depicted in Fig. 4.7, the controller has been designed in order to obtain a phase margin of $\varphi_m = 80°$ at a crossover frequency $\omega_c = 2000\, rad/s$ lower than $\omega_0 = 5454\, rad/s$, which provokes a multiple crossing of the 0dB level, for which the phase margin can be less than the desired one or even negative.

A ω_0 far lower than ω_c (then for a high value of the product LC_o) could cause a low gain margin at frequencies lower than ω_c.

Nevertheless, as already mentioned, the real limit of all the boost-derived converters, consists of the RHPZ of the transfer function G_{vd}, defined in (4.9). As showed in (4.9) and in Fig. 4.5, the value of ω_{RHP} depends on the load power/resistance and on the L inductance value. From a time domain point of view, the RHPZ can be observed from the v_{C_o} output voltage dynamical response in opposition to d input variation. Indeed, if the duty cycle d is stepped at a higher value, the conduction period of the high switch S_2 within the switching period T_s is reduced, and the C_o capacitance start discharging through the load, until the L inductor current increases enough to provide the necessary power (hence the dependences from L and R). If, for example, in a controlled converter, the demanded load power increases, the output voltage instantaneously decreases, because the output capacitor C_o has to provide

a negative current. The controller will try to restore the output voltage by increasing the duty cycle. As mentioned above, because of the response of v_{C_o} in opposition with the duty d variation, if the controller reaction is too fast compared to the charging capability of the inductor L, the inductor current i_L is not able to provide to C_o the necessary charge to restore the output voltage v_{Co}. Hence, a further increase of the duty cycle value d leads to a further reduction of the output voltage v_{C_o}, which could result in instability.

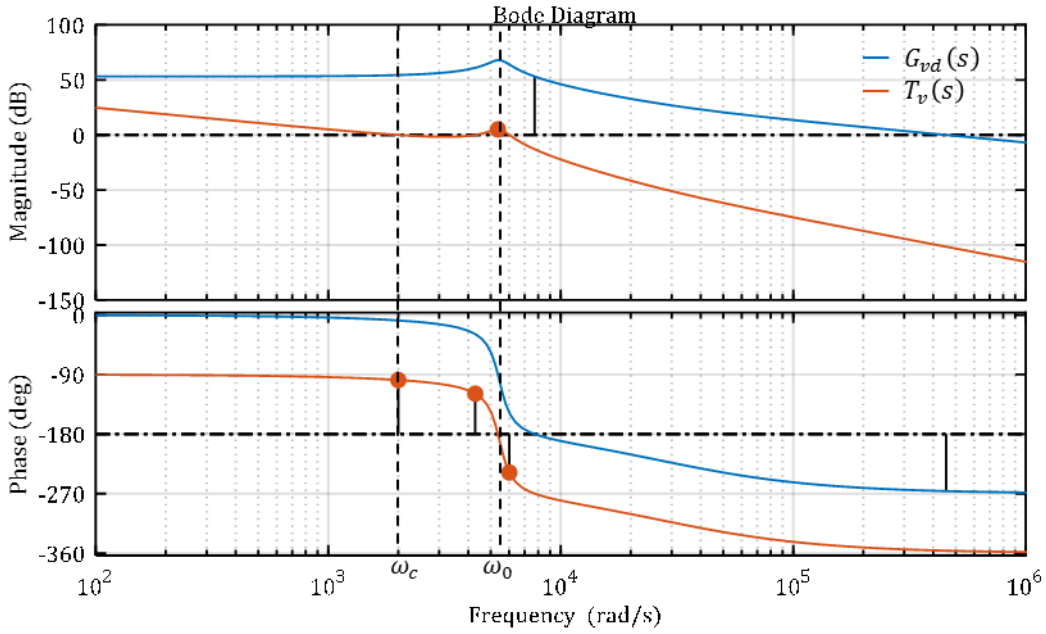


Fig. 4.7 Bode plot of the G_{vd} transfer function and open-loop function T_v of the single loop controlled system, with $\omega_0 = 5454 rad/s$ and $\omega_c = 2000 rad/s$ ($L = 200\mu H$, $C_o = 100\ \mu F$, $V_o = 350V$, $V_{in} = 270V$ and $R = 10\Omega$).

The negative phase amount due to the RHPZ makes pretty challenging the realization of a controller with a ω_c value at high frequencies as wished with a satisfying phase margin. The only easy way to avoid the negative phase contribution of the RHPZ consists of pushing it at frequencies higher than the desired crossover frequency ω_c.

A small value of inductance L could bring a large benefit in terms of stability because the charging/discharging process of the inductor would be faster, hence the ω_{RHP} value results higher, as can be deduced from (4.9). As observed in the previous chapter, the L inductance value is strictly related to the current ripple requirements and the input filter size, along with the choice of the switching frequency f_s, hence the choice of a smaller value of L should be considered along with all the relative design choices. The alternative consists in choosing a different control strategy.

In the domain of the linear control strategies, a double loop strategy control, as showed in Fig. 4.8, is often preferred to overcome the combined effect of the double complex poles pair with pulsation ω_0 and the RHPZ.

Furthermore, the regulation of the input current is a desirable feature, especially for middle and high power applications, since it allows to control possible current surge or excursion that could damage the converter components.

The controlled variable is the inductor current i_L. That implies the employ of an additional probe and its conditioning network to ensure a proper measurement. Nevertheless, the inner loop adds several benefits to the closed-loop transfer function. The inductor control-to-current transfer function G_{id} is obtained from (4.7):

$$G_{id}(s) = \left.\frac{i_L(s)}{d(s)}\right|_{v_{in}=0, i_o=0} = \frac{2\,V_o}{R(1-D)^2}\,\frac{\left(1+\frac{s\,R\,C_o}{2}\right)}{1+s\frac{2\zeta}{\omega_0}+\frac{s^2}{\omega_0}} \tag{4.15}$$

Clearly, the $G_{id}(s)$ shows the same poles as the $G_{vd}(s)$ function in (4.8). Though, it is worth remarking the absence of the RHPZ in the function numerator. The phase of the G_{id} function indeed has a more convenient profile, as shown in Fig. 4.9.

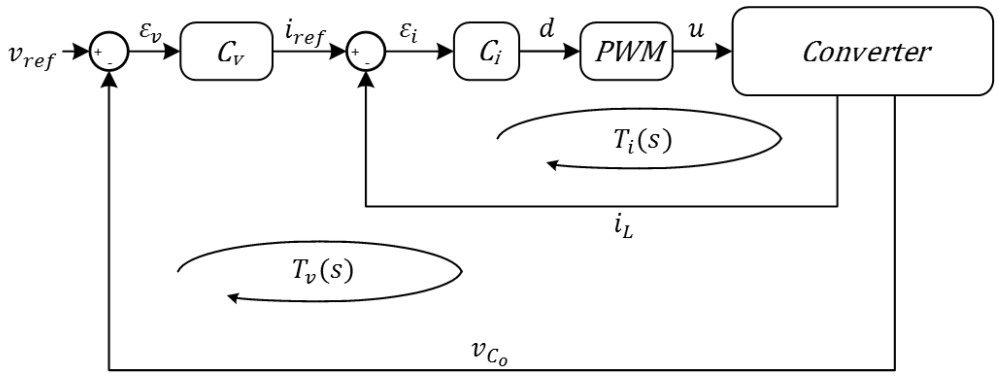


Fig. 4.8 Double loop control scheme.

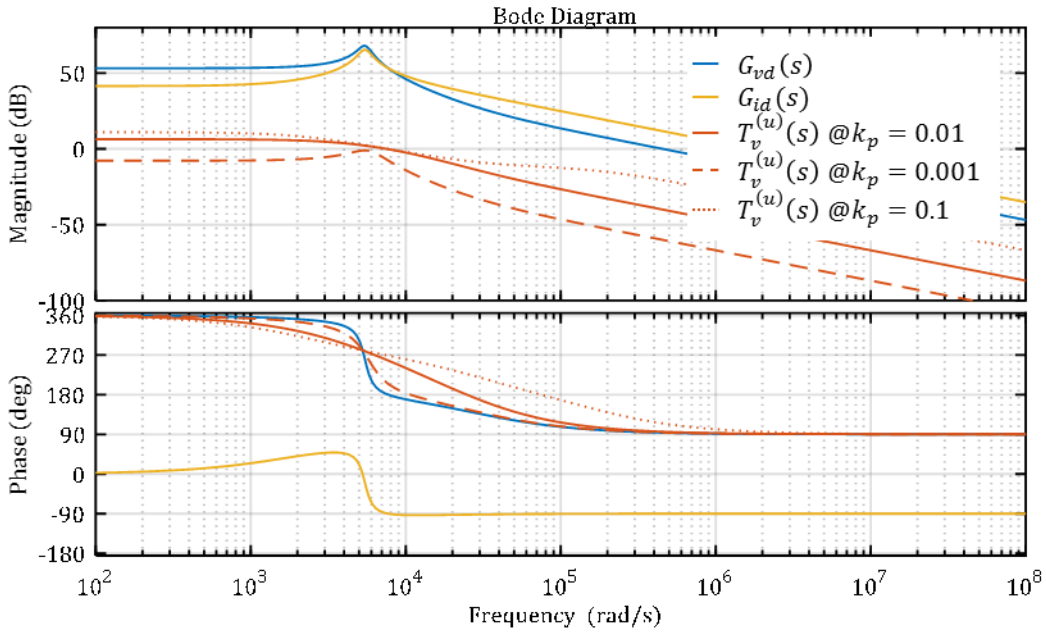


Fig. 4.9 Comparison between the open loop control-to-output transfer function G_{vd}, the open loop control-to-current transfer function G_{id} and the uncompensated open loop transfer function $T_v^{(u)}$ controlled by a proportional P regulator ($k_p = 0.1, 0.01, 0.001$, $L = 200\mu H$, $C_o = 100\ \mu F$, $V_o = 350V$, $V_{in} = 270V$ and $R = 10\Omega$).

Indeed, not being limited from any RHPZ, the crossover frequency of the transfer function $T_i(s)$ can be chosen at frequencies arbitrarily high by a simple PI controller, where $T_i(s)$ is the open-loop transfer function of the inner loop as showed in Fig. 4.8:

$$T_i(s) = \frac{i_L(s)}{\varepsilon_i(s)}\bigg|_{v_{in}=0, i_o=0} = G_{id}(s)\, C_i(s) \tag{4.16}$$

with $C_i(s)$ as the Laplace function of the current controller in Fig. 4.8. In the following analysis, a simple proportional controller ($C_i = k_p$) for the current regulation is used, especially because of its similarities with the peak-current controller, as it will be shown in Section 4.4.1.

In order to compare the single loop and the double loop control strategies, respectively schematized in Fig. 4.6 and Fig. 4.8, it is possible to analyse the G_{vd} transfer function (for the single loop strategy) and the non-controlled open loop transfer function $T_v^{(u)}$ (for the double loop strategy), defined as:

$$T_v^{(u)}(s) = \frac{v_o(s)}{i_{ref}(s)}\bigg|_{v_{in}=0, i_o=0} = \frac{G_{vd}(s) C_i(s)}{1 + T_i(s)} \tag{4.17}$$

In Fig. 4.9, the transfer function $T_v^{(u)}(s)$ exhibits a better phase profile than the $G_{vd}(s)$ one. Indeed, the current regulation causes the *pole splitting* of the complex conjugated poles of G_{vd} in ω_0.

The movement of the poles of the closed loop transfer function $T_i^{(cl)}(s)$ as function of the gain value k_p of the inner loop proportional controller $C_i(s)$ (Fig. 4.8) is showed in the root locus graph in Fig. 4.10, where $T_i^{(cl)}(s)$ is defined as:

$$T_i^{(cl)}(s) = \frac{i_L(s)}{i_{ref}(s)}\bigg|_{v_{in}=0, i_o=0} = \frac{T_i(s)}{1 + T_i(s)} \tag{4.18}$$

$T_i^{(cl)}(s)$ and $T_v^{(u)}(s)$ are the transfer functions which relate state variables of the same system (open voltage loop and closed current loop) to the reference signal i_{ref}, then they have the same poles. Hence, the root locus shown in Fig. 4.10 represent the poles movement of $T_v^{(u)}(s)$ as well.

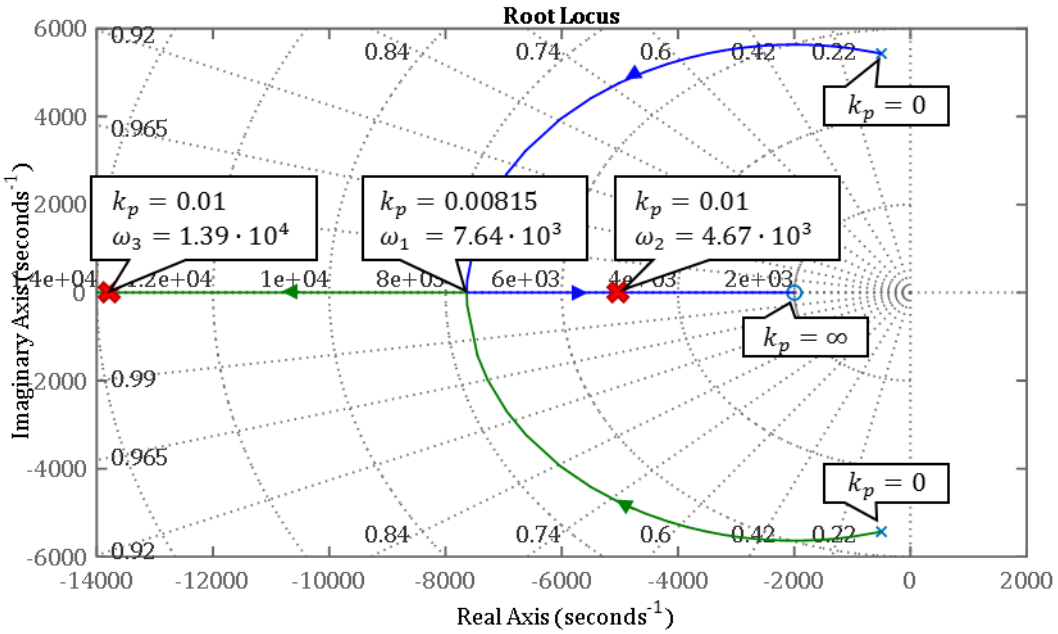


Fig. 4.10 Root locus of the current closed loop transfer function $T_i^{(cl)}(s)$ ($L = 200\mu H, C_o = 100\ \mu F, V_o = 350V$, $V_{in} = 270V$ and $R = 10\Omega$)..

A simple proportional current controller splits the two poles, bringing one toward the G_{id} zero in (4.15) (at $\omega = 2000\, rad/s$) and another one toward high frequencies, as showed in Fig. 4.10. For instance, for $k_p = 0.00815$, the two poles are coincident and placed on the real axis at $\omega_1 = 7.64 \cdot 10^3 rad/s$. By increasing the k_p value, the poles move in opposite directions on the real axes. For $k_p = 0.01$, the two poles are split into $\omega_2 = 4.67 \cdot 10^3 rad/s$ and $\omega_3 = 1.39 \cdot 10^4 rad/s$. With a pole placed at high frequencies (close to the switching one), the open loop function $T_v^{(u)}(s)$ can be then considered as a first order low pass filter, at least in the frequency range where the bandwidth of the closed-loop system is desirable. Fig. 4.9 shows the bode plots of the $T_v^{(u)}(s)$ function by changing the current controller gain k_p, with a remarkable impact especially in the phase profile.

4.4 Control strategy for power disturbance rejection

One of the main tasks of the feedback control loop consists in immunizing the converter behaviour from external disturbances, such as variations of the load power and of the input voltage. The main intent, for the considered application, is to ensure the normal operation of the DC/DC converter during the output power variations, hence only the load disturbances will be discussed in this chapter.

Since the purpose of this study is to immunize the system from outer disturbances, such as those of the load, a proper control strategy is mandatory.

A double loop control strategy, as the one presented in Fig. 4.8, has a moderate ability to reject load transient variation. Indeed, the current mode controller is considered widely effective to reject the effect of the input voltage disturbances on the output voltage, but the current loop has disruptive effects on the output impedance Z_o of the system, hence on the rejection ability of the load disturbances [93]. The system output impedance Z_o should be properly reduced by compensating the system through the output voltage regulation.

In the case of a motor driver application, the DC/DC converter load is composed of the assembly inverter-motor, which absorbs a load power of $P_o(t)$. The system in (4.4) should be modified as:

$$\begin{cases} L\dfrac{di_L}{dt} = V_{in} - (1-d)\, v_{C_o} \\ C_o\dfrac{dv_{C_o}}{dt} = (1-d)\, i_L - \dfrac{P_o(t)}{v_{C_o}} \end{cases} \tag{4.19}$$

The load current term P_o/v_{C_o} in the C_o capacitor current differential equation in (4.19) should be linearized around the nominal power value P_o. On the other hand, as mentioned in Chapter 2, the power supplied to the actuator block is likely to change during the operating mission profile. The system plant will change along with the required power P_o. A PI voltage controller is designed in order to ensure a certain stability margin and rapidity for a given operating point. That means that, in case of variable load, the open loop transfer function does not show the same crossover frequency and phase margin for the whole operating range of the output power.

In order to ensure the same performances for all the output power values and to deal with fast variation of the output power, in our work it has been implemented an energy controller in the outer loop.

The proposed control algorithm consists into a double loop control, as shown in Fig. 4.11.

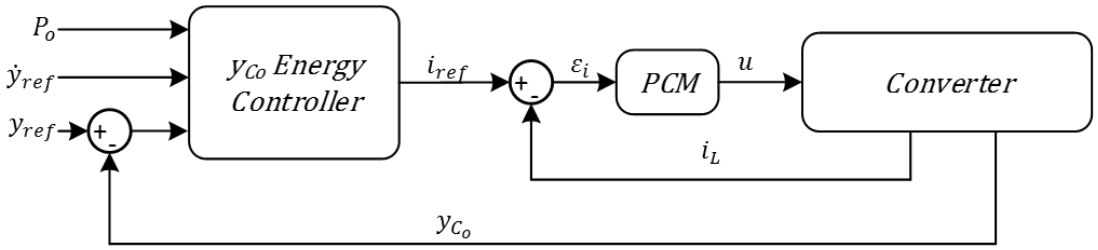


Fig. 4.11 Double loop control scheme, with energy regulation.

4.4.1 Inner Loop: Peak Current Mode Control

In order to obtain a fast response of the current loop, hysteretic regulators are among the most employed in the field of the DC/DC conversion because of their rapidity, robustness and easy implementation. Nevertheless, these regulators suffer of a variable switching frequency, which leads to several difficulties concerning the design of the input filter and the choice of the current ratings of the converter elements [125]. To solve the variable frequency issue, a triggered turn on/off current regulator is usually preferred. The inner current loop, which regulates the main inductor current (i_L), is a peak current mode control (PCM), a robust and widely used controller that ensures many key features [33], [124], [125], such as a fixed switching frequency, a fast dynamic response and an intrinsic over-current protection.

The operating principles of the PCM are illustrated in Fig. 4.12. It consists of a turn-on triggered current controller. The u_1 switch is turned on at the start of each switching period by the trigger signal on the SET terminal of the SR latch. The turn-off signal is provided by the comparator through the RESET terminal when the i_L current reaches the reference signal i'_{ref} defined as:

$$i'_{ref} = i_{ref} + i_{ramp}, \tag{4.20}$$

$$i_{ramp}(t) = m_c\left(\frac{1}{2} - \frac{t}{T_s}\right)T_s, \qquad t \in [m\,T_s, (m+1)T_s], m \in \mathbb{N} \tag{4.21}$$

where i_{ramp} is a saw tooth signal known as compensating ramp, which is employed to damp any perturbations on the i_L current and stabilize the current loop [130], [131], with m_c as the slope value of the ramp in absolute value. Indeed, in order to avoid any sub-harmonic oscillations and chaotic behaviour , the slope compensation is essential for peak-current mode when duty cycle is above $D > 0.5$. Even though $D < 0.5$, it is desirable to add a slope compensation to decrease any noise influence. To avoid any stability issues of the current loop at $D = 1$, the value of the m_c slope should be chosen $m_c > 0.5\,m_2$. A value of slope $m_c = m_2$ can be set to obtain the immediate rejection of the current noise in one cycle period (deadbeat control)[132].

By observing the waveforms in Fig. 4.12(b), it is possible to deduce from (4.20) the mean value of the inductor current i_L in steady state. The following equations are evaluated in steady state at the time $t = D\,T_s$, when the sensed current reaches the reference signal i'_{ref}:

$$< i_L >_{T_s} = i_{ref} + m_c\left(\frac{1}{2} - D\right)T_s - \frac{1}{2}m_1 D\,T_s \tag{4.22}$$

or also

$$< i_L >_{T_s} = i_{ref} + m_c\left(\frac{1}{2} - D\right)T_s - \frac{1}{2}m_2(1-D)\,T_s \tag{4.23}$$

Where the terms m_1 and m_2 are respectively the i_L slopes in absolute value during the charging and the discharging phases of the inductor L, defined as:

$$m_1 = \frac{V_{in}}{L}\,, \qquad m_2 = \frac{V_o - V_{in}}{L} \tag{4.24}$$

Both equations (4.22), (4.23) are employed in [125], [130] to develop the equivalent model of the modulation block of a peak-current controller for the small signal perturbations:

$$d = F_m \left(i_{ref} - i_L - F_v\, v_o\right) \tag{4.25}$$

$$F_m = \frac{f_s}{\frac{1}{2}(m_1 - m_2) + m_c}\,, F_v = \frac{D(1-D)}{2\,L\,f_s} \tag{4.26}$$

The contribution of the term $F_v\, v_o$ in (4.25) can be considered small enough compared to the current error $i_{ref} - i_L$, thus the current peak controller can be assumed as a simple proportional controller with gain F_m, for which the considerations made in Section 4.3.2 are still valid.

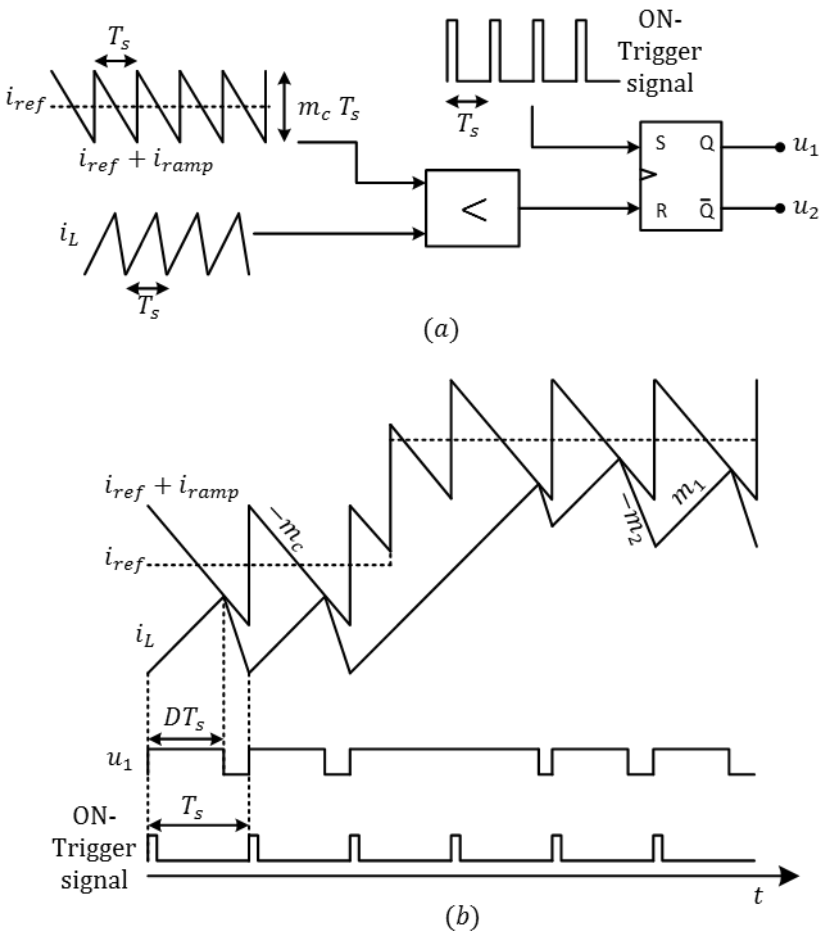


Fig. 4.12 Peak current controller block scheme (a) and waveforms (b).

4.4.2 Energy loop

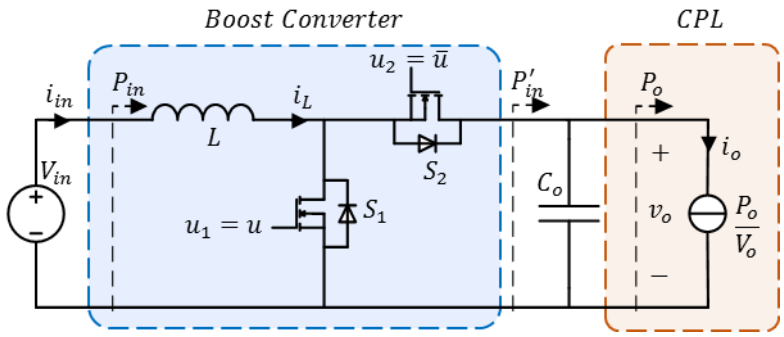


Fig. 4.13 Boost converter.

The outer regulator purpose is to control the output voltage. The proposed controller regulates the energy y_{C_o} stored in the output capacitor C_o, then it controls indirectly the output voltage $v_o = v_{C_o}$. The energy stored in the capacitor is defined as:

$$y_{C_o} = \frac{1}{2} C_o v_{C_o}^2 \tag{4.27}$$

The error between the controlled variable y_{C_o} and its reference y_{ref} is defined as:

$$\varepsilon_{y_{C_o}} = y_{ref} - y_{C_o}, \qquad y_{ref} = \frac{1}{2} C_o V_o^2 \tag{4.28}$$

with $v_{ref} = V_o$ as the reference value of the output voltage.

The energy regulator in Fig. 4.11 sets the dynamic behaviour of the error $\varepsilon_{y_{C_o}}$ by means of a proportional and an integrator term through the following control law:

$$\dot{\varepsilon}_{y_{C_o}} + k_p \varepsilon_{y_{C_o}} + k_i \int \varepsilon_{y_{C_o}} \, dt = 0 \tag{4.29}$$

The time derivative of (4.29) provides the second order equation:

$$\ddot{\varepsilon}_{y_{C_o}} + k_p \, \dot{\varepsilon}_{y_{C_o}} + k_i \varepsilon_{y_{C_o}} = 0 \tag{4.30}$$

The constant values k_p and k_i are chosen by the designer to force the dynamical evolution of the error $\varepsilon_{y_{C_o}}$:

$$k_p = 2\,\zeta \omega_e, \qquad k_i = \omega_e^2 \tag{4.31}$$

where ζ and ω_e are respectively the damping factor and the cut-off angular frequency of the controlled system.

By referring to Fig. 4.13, the energy variation in the output capacitor C_o is given by:

$$\dot{y}_{C_o} = C_o v_{C_o} \frac{dv_{C_o}}{dt} = P'_{in} - P_o \tag{4.32}$$

In (4.32), the term P'_{in} represents the power flow upstream the output capacitor C_o and P_o is the power supplied to the CPL.

It is purposely assumed that the converter is lossless and that the magnetic energy stored by the inductor L is negligible compared to the electrostatic energy stored in C_o (which is reasonable for high efficiency converters for HVDC applications):

$$\frac{1}{2}C_o V_o^2 \gg \frac{1}{2}L\, I_L^2 \tag{4.33}$$

Under this hypothesis, the power flow can be approximated to the input power supplied to the boost converter $P'_{in} \cong P_{in}$ [133], [134], then:

$$\dot{y}_{C_o} = P'_{in} - P_o \cong P_{in} - P_o \tag{4.34}$$

The choice of controlling the stored energy y_{C_o} allows obtaining the linear relation (4.34) between the controlled variable y_{C_o} and the output power P_o.

As already mentioned for the average model approximation, in order to uncouple the stored energy dynamical behaviour and the energy exchange process at the switching frequency, ω_e should be chosen lower enough than the switching angular frequency $\omega_{f_s} = 2\,\pi\, f_s$. If the bandwidth of the inner controller higher enough than the energy controller bandwidth ω_e, in the frequency range in which the energy regulator operates, the dynamic of the inductor current i_L can be assimilated with the dynamic of its reference i_{ref}:

$$i_{in} = i_L \cong i_{ref} \tag{4.35}$$

Then P_{in} in (4.34) can be replaced by:

$$P_{in} \cong V_{in}\, i_{ref} \tag{4.36}$$

The reference value for the inner current loop is derived from (4.29) through (4.28), (4.34) and (4.36):

$$i_{ref} = \frac{P_o + \dot{y}_{ref} + k_p\,.\,\varepsilon_{y_{C_o}} + k_i \int \varepsilon_{y_{C_o}}\,.\,dt}{V_{in}} \tag{4.37}$$

The equivalent scheme of the energy controller for the generation of the reference signal i_{ref} is detailed in the following figure.

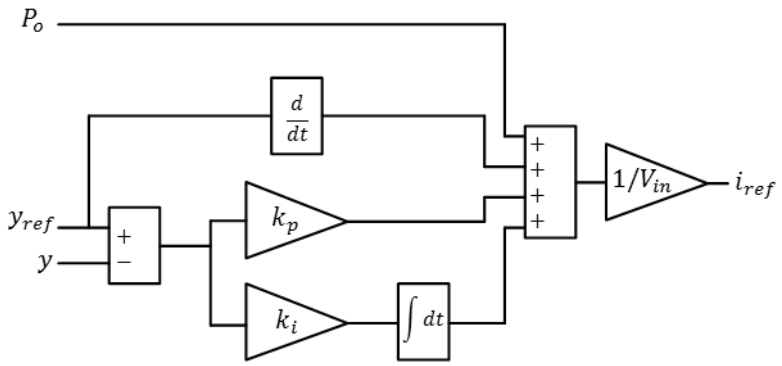


Fig. 4.14 Energy controller scheme.

The P_o term in (4.37) makes the outer controller more sensitive to the variation of the load power, compared to a classical PI voltage regulator. It allows a fast response to the output power P_o variation and avoid to overload the integrator term of the PI controller. Nonetheless, it also implies a high

sensitivity to noise measurement. It is possible to compare the ability of the energy and PI controllers to reject the power variation by analysing the small signal model of the closed loop system. By gathering and linearizing the converter average equations in (4.19) and the control law in (4.25), (4.37), the system becomes:

$$\begin{cases} L\dfrac{d\tilde{\imath}_L}{dt} = \tilde{v}_{in} - (1-D)\tilde{v}_{C_o}(t) + \tilde{d}\,V_o \\ C_o\dfrac{d\tilde{v}_{C_o}}{dt} = (1-D)\tilde{\imath}_L + \tilde{d}\,I_L + \dfrac{P_o}{V_o^2}\tilde{v}_{C_o} - \dfrac{\tilde{p}_o}{V_o} \\ \tilde{d} = F_m\left(\tilde{\imath}_{ref} - \tilde{\imath}_L - F_v\,\tilde{v}_{C_o}\right) \\ \tilde{\imath}_{ref} = C_{PI}\left(\tilde{v}_{ref} - \tilde{v}_{C_o}\right) \;\; or \;\; C_{energy}\left(\tilde{v}_{ref} - \tilde{v}_{C_o}\right) \end{cases} \tag{4.38}$$

Where $\tilde{p}_o$ is the small signal perturbation of the output power P_o, $\tilde{\imath}_{ref}$ is the current reference perturbation, $\tilde{v}_{ref}$ is the voltage reference perturbation, C_{PI} is the PI voltage controller transfer function and C_{energy} is the energy controller transfer function. Their Laplace forms can be expressed as follows:

$$C_{PI}\left(v_{ref}(s) - v_{C_o}(s)\right) = \left(k_p^{(PI)} + \frac{k_i^{(PI)}}{s}\right)\left(v_{ref}(s) - v_{C_o}(s)\right), \tag{4.39}$$

$$\begin{aligned} &C_{energy}\left(v_{ref}(s) - v_{C_o}(s)\right) \\ &= \frac{1}{V_{in}}\left(p_o(s) + s\,C_oV_o\,v_{ref}(s) + C_oV_o\left(k_p^{(Energy)} + \frac{k_i^{(Energy)}}{s}\right)\left(v_{ref}(s) - v_{C_o}(s)\right)\right) \end{aligned} \tag{4.40}$$

In Fig. 4.15, the transfer functions which characterize the perturbation of the output voltage as function of the output power disturbance are compared, in order to show the output power disturbance rejection of the systems when the two controllers are implemented, defined as:

$$G_{vp}(s) = \left.\frac{v_{C_o}(s)}{p_o(s)}\right|_{v_{in}=0, v_{ref}=0} \tag{4.41}$$

The controllers are designed in order to achieve a bandwidth of 2.5 k rad/s ($\omega_e = 2.5\text{k rad/s}$ and $\zeta = 0.7$ in (4.31)) with both controllers C_{energy} and C_{PI}.

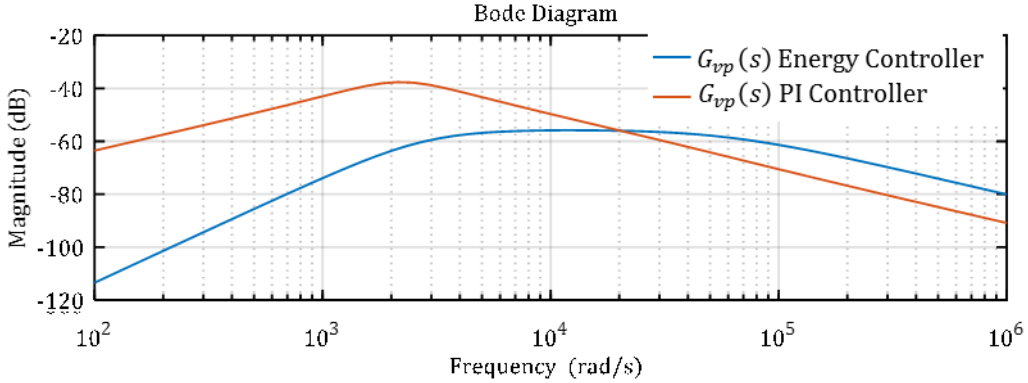


Fig. 4.15 G_{vp} power-to-output transfer function for a double loop control strategy with PI and energy regulator.

The G_{vp} magnitude is lower when the outer loop of the system is compensated through an energy controller, which means that the ability to reject the output power disturbances is clearly better when the energy controller is employed.

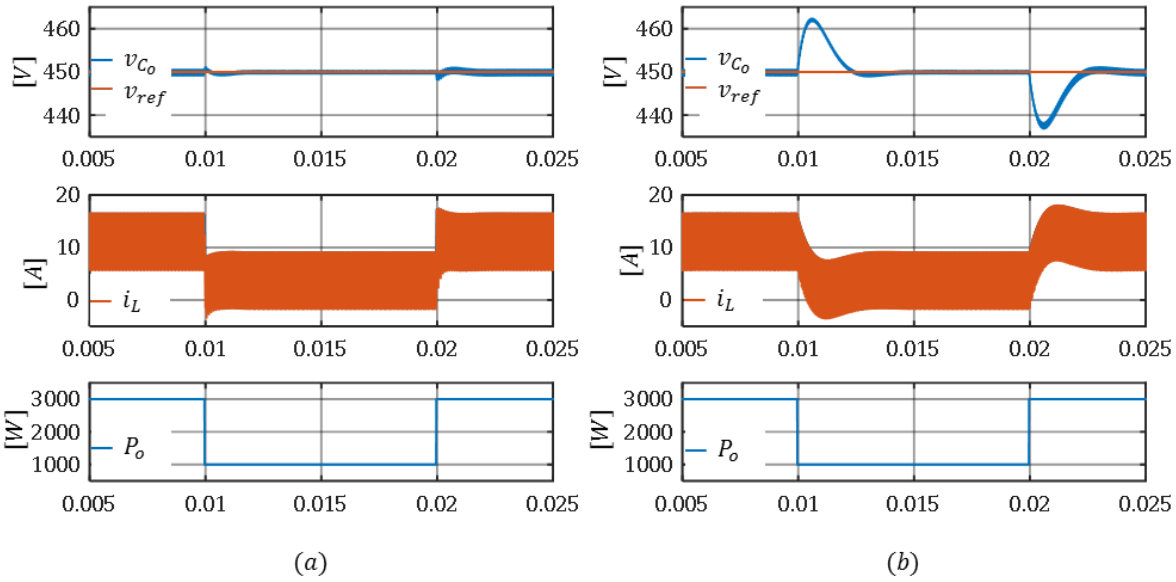


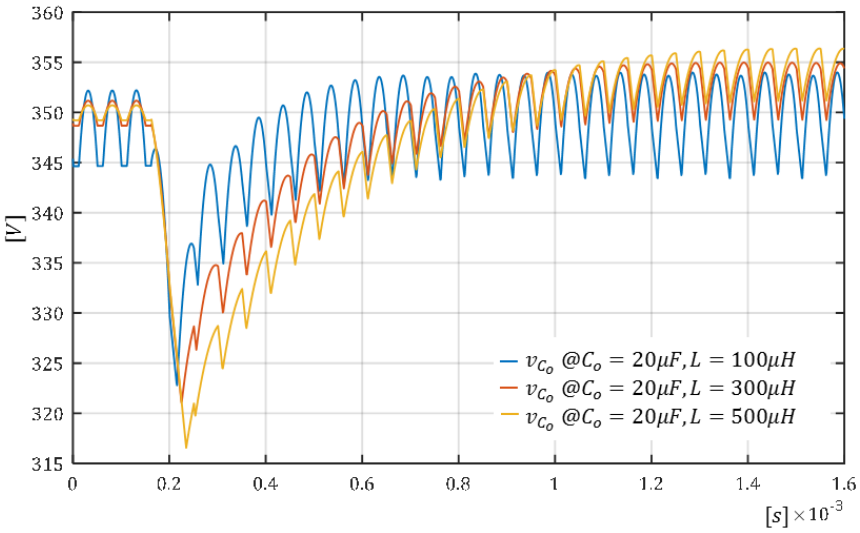
Fig. 4.16 Circuital simulation waveforms in case of a step-down and step-up load transient with the energy controller C_{energy} (a) and with the PI voltage controller C_{PI} (b) ($L = 500\mu H, C_o = 100\ \mu F, V_o = 450V, V_{in} = 270V$, $P_o = 1kW \leftrightarrow 3kW, \omega_e = 2.5k\frac{rad}{s}, \zeta = 0.7, f_s = 20kHz$).

Indeed, as showed in Fig. 4.15, for the low range of frequencies (up to $\sim f_s/10 = 2kHz$), then the whole frequency range below the controller bandwidth ω_e, the amplitude of the G_{vp} transfer function is far higher for the system controlled by the simple voltage PI, which implies more important excursion of the output voltage. That is confirmed in Fig. 4.16, where a load power step of $P_o = 1kW \leftrightarrow 3kW$is simulated for the system controlled with both control strategies. In Fig. 4.16(b), it is possible to observe a slower reaction to the power variation of both output voltage and inductor current when the voltage output is controlled, with a consequent larger overshoot and undershoot values of v_{C_o}. On the other hand, it should be remarked that the energy controller requires the direct measure of the load power P_o, which implies an increased sensitivity to the noise and other measurement related issues, as it will be shown in the experimental results in Chapter 5.

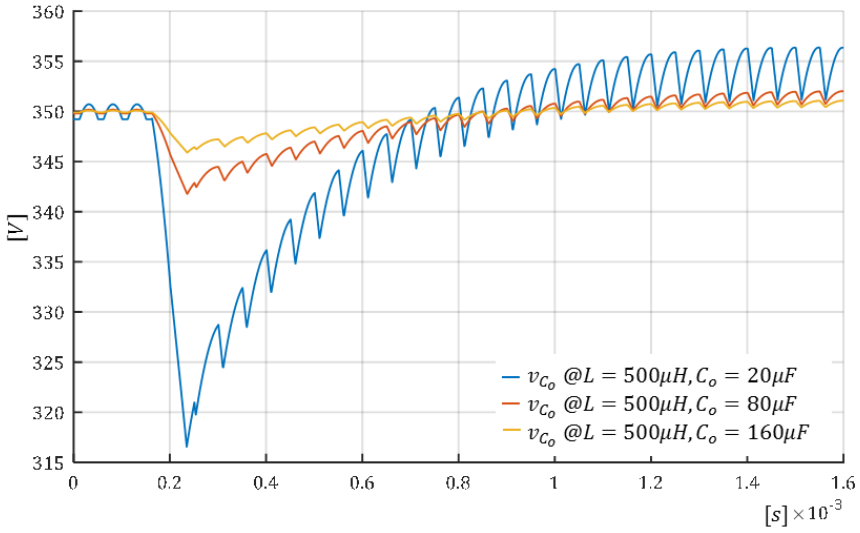
4.5 Capacitor design for load transient rejection

It is clear that the dynamic behaviour is directly determined by the control strategy and the performances of the regulators. Nevertheless, due to the practical limitation of the regulators and the modulation blocks (duty cycle saturation, finite bandwidth), the transient behaviour of the system state variables cannot be minimized beyond a certain limit by the control strategy. The transient response is determined by the passive components (L and C_o), the control strategy and its parameters, whose combination defines the profile of the output impedance Z_o of the closed loop system (G_{vp} for the output power disturbance transfer function). It has been remarked in the previous sections that the passive components values can impact on the stability of the system, as for RHPZ issue. The output impedance (or the transfer function G_{vp} in the considered case) frequency profile (Fig. 4.15) cannot be shaped at will by the control strategy, and shows a certain dependency on the inductance and capacitance values

of the passive components. The following Fig. 4.17 show the impact of the variation of the passive components on the output voltage v_{C_o} response to a step variation of the load power P_o for a system controlled as in Fig. 4.11.



(*a*)



(*b*)

Fig. 4.17 Step response of the output voltage v_{C_o} to the power load transient ($V_o = 350V$, $V_{in} = 270V$ and $P_o = 0 \rightarrow 3000W$), by varying L (a) and C_o(b) of a boost converter controlled as in Fig. 4.11.

Even if the controller parameters are designed to ensure the same bandwidth of the closed loop ($\varphi_m = 53°$ and $\omega_e = 1.25\ k\ rad/s$), the output voltage exhibits different settling times and overshoot values depending on the C_o and L values.

The converter should usually respect the voltage specifications at the output terminals required by the application, whatever the variation of its operating point (reference tracking or disturbance rejection). In the considered case, the output voltage variation should be kept within a voltage range $\Delta v_{lim}^{(LT)}$, which ensures the controllability of the cascade inverter which supplies the motor.

During a large variation of the operating point, depending on the controller topology and its bandwidth, the capacitor could sustain a large amount of current and exhibit a voltage spike that could exceeds the consented limits. Hence, in case of fast transition of the load current, the capacitor design conditions

could be more constraining than the steady state case. In this section, the minimal value of capacitance is deducted to guarantee that the voltage excursion during abrupt transition of the power load does not exceed the specification range $\Delta v_{lim}^{(LT)}$. The analysis is conducted in the time domain for a load power step up and a step down transitions ΔP_o:

$$\Delta P_o = P_o^{(high)} - P_o^{(low)}, \tag{4.42}$$

where $P_o^{(high)}$ and $P_o^{(low)}$ are the high and low values of output power, respectively.
An approach is developed to approximately deduce the capacitance value for smooth load transient too.

4.5.1 Evaluation of the minimal value of C_o in step-up load transient conditions

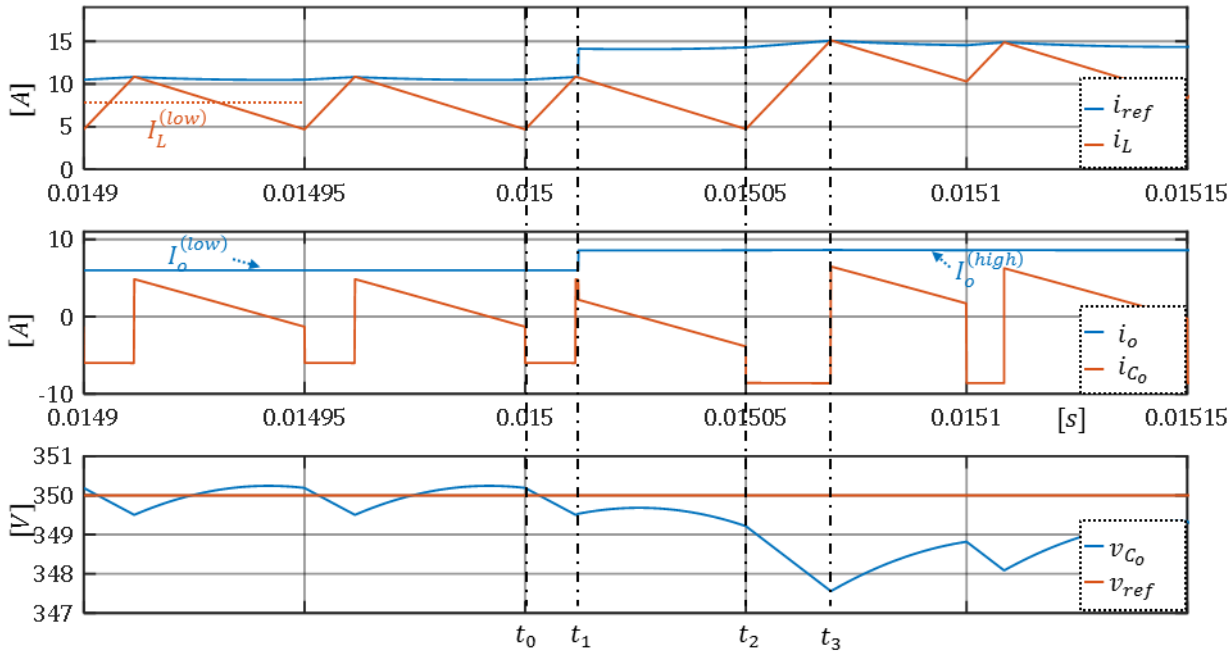


Fig. 4.18 Step-up load transient, simulation waveforms (L=500μH, $V_{in} = 270V, V_o = 350V, C_o = 100\mu F$, $f_s = 20\ kHz$, $P_o = 3kW, \Delta P_o = 0.3\ P_o$).

During a sudden increase of the load power from its lowest value $P_o^{(low)}$ to a higher value $P_o^{(high)}$, the reference current generated by the outer loop, abruptly increases (Fig. 4.18) because of the P_o term in the control law (4.37).

In the following analysis the condition $u = 1{,}0$ represents the conduction state of the switch S_1 (on→ 1, off→ 0) in Fig. 4.13, hence the complementary one of the S_2 switch state.

The following notations $I_o^{(low)}$, $I_L^{(low)}$ and $I_o^{(high)}$, $I_L^{(high)}$ represent the output load and the L inductor steady-state average currents respectively at low load power $P_o^{(low)}$ and high load power $P_o^{(high)}$. If the voltage excursion is not excessive, then the output current waveform can be assumed as a step function, as shown in Fig. 4.18, with a step amount of:

$$\Delta I_o = I_o^{(high)} - I_o^{(low)} = \Delta P_o / V_o \tag{4.43}$$

The worst case is considered, i.e. when the load transient occurs in $t = t_1$, just after the turn-off of the switch S_1. In this case, the inductor current i_L is too low to supply the load, and it will not start rising before $t = t_2$, at the beginning of the next switching period. The load current is only provided by the output capacitor C_o, which causes the undershoot of its voltage v_{C_o}.

The analytical expressions of the inductor and capacitor currents (i_L and i_{C_o}) for $t \in [t_0, t_3]$ are given below:

$$\begin{cases} i_L = I_L^{(low)} - \Delta i_L \left(\frac{1}{2} - f_s \frac{(t - t_0)}{D} \right) \\ i_o = I_o^{(low)} \\ i_{C_o} = -i_o \end{cases} \quad t \in [t_0, t_1], u = 1 \tag{4.44}$$

$$\begin{cases} i_L = I_L^{(low)} + \Delta i_L \left(\frac{1}{2} - f_s \frac{(t - t_1)}{1 - D} \right) \\ i_o = I_o^{(high)} \\ i_{C_o} = -i_o + i_L \end{cases} \quad t \in [t_1, t_2], u = 0 \tag{4.45}$$

$$\begin{cases} i_L = I_L^{(low)} - \Delta i_L \left(\frac{1}{2} - f_s \frac{(t - t_2)}{D} \right) \\ i_o = I_o^{(high)} \\ i_{C_o} = -i_o \end{cases} \quad t \in [t_2, t_3], u = 1 \tag{4.46}$$

For $t \in [t_2, t_3]$, the switch S_1 stays in on-state ($u_1 = 1$) until the inductor current i_L reaches its reference value i_{ref}, as shown in Fig. 4.18. During this sequence $i_{C_o} = -I_o^{(high)}$, then the output voltage v_{C_o} decreases. As mentioned above, the worst case occurs when the load transient happens just after S_1 turned off at $t = t_1$. In this case, the inductor current resumes increasing only at the end of the switching period $t = t_2$, then after $D'T_s$, and it reaches its reference at t_3, so the switch S_2 starts conducting and the inductor current flows toward C_o. The minimum value of v_{C_o} is then reached exactly at t_3. The instant t_3 is computed by solving the 4th degree equation $i_L = i_{ref}$ from (4.46) and (4.37) as function of C_o:

$$I_L^{(low)} - \Delta i_L \left(\frac{1}{2} - \frac{f_s (t_3 - t_2)}{D} \right) = \frac{P_o^{(high)} + \frac{1}{2} C_o k_p \left(V_o^2 - \left(v_{C_o}(t_3) \right)^2 \right) + \frac{1}{2} C_o k_i \int_0^{t_3} \left(V_o^2 - \left(v_{C_o}(\tau) \right)^2 \right) d\tau}{V_{in}} \tag{4.47}$$

where

$$v_{C_o}(t) = v_{C_o}(t_0) + \frac{1}{C_o} \int_{t_0}^{t} i_{C_o}(\tau)\, d\tau \tag{4.48}$$

In steady state, the reference current i_{ref} is equal to the peak value of the current i_L. From (4.37), the initial value (before the load transient at $t = t_1$) of the integral term in (4.47) can be then deducted as:

$$\frac{1}{2}C_o k_i \int_0^{t_1}\left(V_o^2-\left(v_{C_o}(\tau)\right)^2\right)d\tau=\frac{V_{in}\,\Delta i_L}{2}-\frac{1}{2}C_o k_p\left(V_o^2-v_{C_o}^2(t_1)\right)\approx\frac{V_{in}\,\Delta i_L}{2} \tag{4.49}$$

The proportional term in (4.47) is negligible in steady state. Such approximation allows to explicitly solve (4.47) for t.

The voltage excursion results:

$$\Delta v_{C_o}=\left|v_{C_{o_{max}}}-v_{C_o}(t_3)\right|<\Delta v_{lim}^{(LT)} \tag{4.50}$$

where $v_{C_{o_{max}}}$ is the maximal v_{C_o} value in steady-state, calculated in Chapter 3, Section 3.4.2. The minimum value of v_{C_o} is evaluated as in (4.48). The minimal value of C_o to contain the undershoot under the admissible limit is obtained when $\Delta v_{C_o}=\Delta v_{lim}^{(LT)}$.

4.5.2 Evaluation of the minimal value of C_o in step-down load transient conditions

Similar considerations may be applied for the overshoot case, when the load power quickly steps down from $P_o^{(high)}$ to $P_o^{(low)}$. With a dual discussion, a C_o value for the step-down load transient case can be determined.

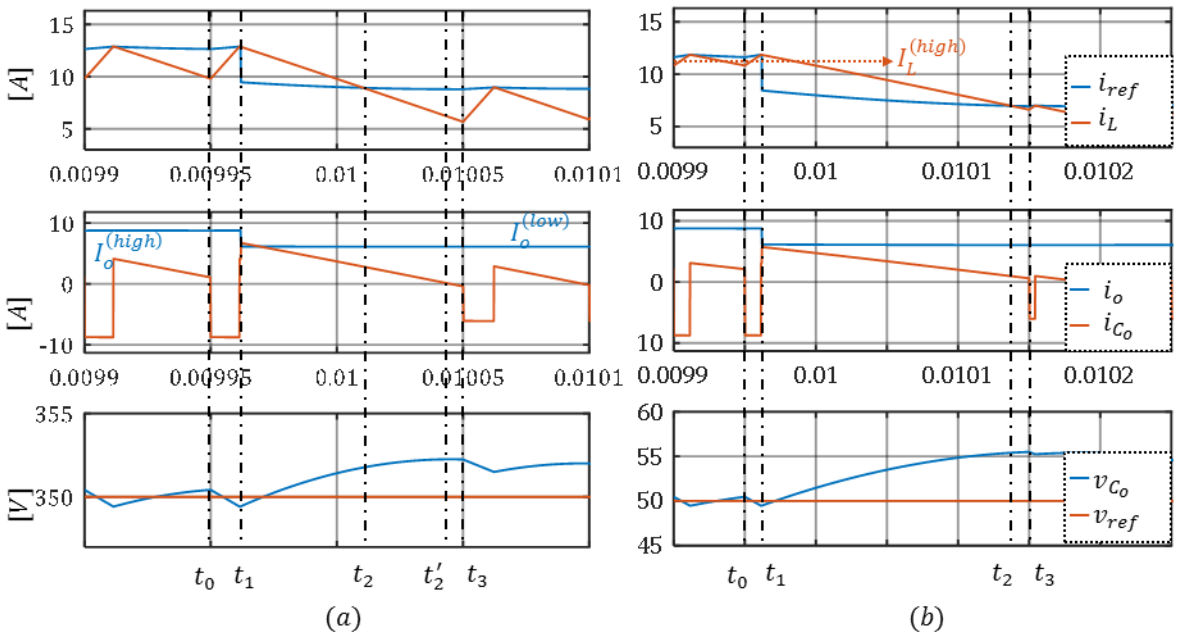


Fig. 4.19 Step-down load transient, simulation waveforms ($V_{in}=270V, V_o=350V, C_o=100\mu F$, $f_s=20\ kHz$, $P_o=3kW, \Delta P_o=0.3\ P_o$) with L=3mH (a) and L=2mH (b).

When the P_o load power step occurs at $t=t_1$, referring to Fig. 4.19(a) and (b), the reference current i_{ref} drops down. In both figures, the i_L current reaches its reference at $t=t_2$, but the switch S_2 conducts until the following trigger signal of the PCM controller at $t=t_3$. During the period $t\in[t_1,t_3]$, the inductor current charges the C_o capacitor. The analytical expressions of the currents time domain waveforms can be written as:

$$\begin{cases} i_L = I_L^{(high)} + \Delta i_L \left(-\frac{1}{2} + f_s \frac{(t - t_0)}{D} \right) \\ i_o = I_L^{(high)} \\ i_{C_o} = -i_o \end{cases} \qquad t \in [t_0, t_1], u = 1 \tag{4.51}$$

$$\begin{cases} i_L = I_L^{(high)} + \Delta i_L \left(\frac{1}{2} - f_s \frac{(t - t_1)}{1 - D} \right) \\ i_o = I_o^{(low)} \\ i_{C_o} = -i_o + i_L \end{cases} \qquad t \in [t_1, t_3], u = 0 \tag{4.52}$$

The time t_2 can be evaluated, as for the undershoot case, by equalizing $i_L = i_{ref}$ from (4.37) and (4.52), and solving for t:

$$I_L^{(high)} + \Delta i_L \left(\frac{1}{2} - f_s \frac{(t - t_1)}{1 - D} \right) = \\ = \frac{P_o^{(low)} + \frac{1}{2} C_o k_p \left(V_o^2 - \left(v_{C_o}(t_2) \right)^2 \right) + \frac{V_{in} \Delta i_L}{2} + \frac{1}{2} C_o k_i \int_{t_1}^{t_2} \left(V_o^2 - \left(v_{C_o}(\tau) \right)^2 \right) d\tau}{V_{in}} \tag{4.53}$$

Two cases should be distinguished. The voltage v_{C_o} exhibits a parabolic waveform. Then, the overshoot could occur when the current through C_o becomes negative (i.e. when the time derivative of v_{C_o} is zero at $t = t_2'$ in Fig. 4.19(a)) or at the end of the conduction of S_2 ($t = t_3$ in Fig. 4.19(b)), if the trigger signal of S_1 occurs before than v_{C_o} reaches its peak value.

The first case is depicted in Fig. 4.19(a). The overshoot instant t_2' can be easily found by setting $i_{C_o} = 0$ in (4.52).

If i_L reaches the i_{ref} reference and S_1 starts conducting before i_L turns negative, the output voltage v_{C_o} exhibits its maximum value at the end of the switching period, in $t = t_3$, as shown in Fig. 4.19(b).

The overshoot time is given by rounding the time t_2 to the closest multiple of the switching period:

$$t_3 = T_s \, ceil\left(\frac{t_2}{T_s} \right) \tag{4.54}$$

The condition which determines the voltage maximum value, can be expressed as:

$$v_{C_{o max}} = \begin{cases} v_{C_o}(t_3), & t_2' > t_3 \\ v_{C_o}(t_2'), & t_2' \le t_3 \end{cases} \tag{4.55}$$

As for the undershoot case, the minimal value of C_o to contain the undershoot under the admissible limit is obtained by solving in C_o the following equation:

$$\Delta v_{C_o} = \left| v_{C_{o min}} - v_{C_{o max}} \right| = \Delta v_{lim}^{(LT)} \tag{4.56}$$

where $v_{C_{o_{min}}}$ is the minimal value of v_{C_o} in steady state, evaluated in Chapter 3, Section 3.4.2.

4.5.3 Evaluation of the minimal value of C_o for a smooth load transient condition

Contrary to the aforementioned case, in most applications the load variation is not instantaneous, but exhibits a limited dynamic evolution, which leads to lower undershoot and overshoot values of the output voltage. For less stringent load power profiles a smaller capacitance C_o is needed. In order to design C_o with the same approach employed for the instantaneous load transient, an equivalent fictive load power step is defined, which leads to the same output voltage undershoot or overshoot caused by the real profile of the load power.

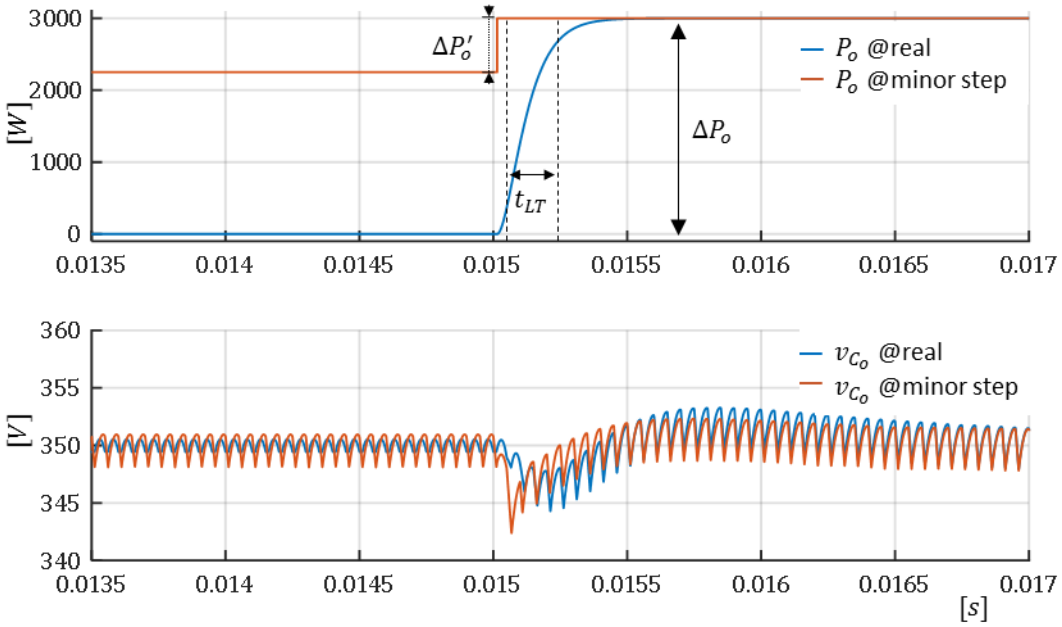


Fig. 4.20 Output voltage v_{C_o} simulation waveforms with a smooth load transient and an equivalent minor instantaneous step ($V_{in} = 270V, V_o = 350V, Co = 27.4\mu F,\ \omega_e = 2.5k\frac{rad}{s}, t_{LT} = 200\mu s, L = 500\mu H, f_s = 20kHz, N_{LT} = 4$).

The smooth load evolution has been assumed as a step response to a second order low pass filter, with transition time t_{LT} between 10% and 90% of the variation, as shown in Fig. 4.20.

Then, the finite integer number N_{LT} is the number of switching periods occurring during the load transient interval t_{LT} (rounded to the greater integer) according to (4.57) and, finally, the amplitude $\Delta P_o'$ of the fictive load step is determined by dividing the maximal variation ΔP_o of the real load power by N_{LT}:

$$N_{LT} = ceil(t_{LT} f_s) \tag{4.57}$$

$$\Delta P_o' = \frac{\Delta P_o}{N_{LT}} \tag{4.58}$$

Fig. 4.20 shows the output voltage waveforms obtained during a real ΔP_o load transient (from 0 to P_o) with low dynamic (blue curves) and a fictive power step (red curves) of amplitude $\Delta P_o'$ (from $P_o - \Delta P_o'$ to P_o) defined in (4.58); the output voltage v_{C_o} exhibits the same undershoot in both cases. In conclusion,

for low dynamic load power profiles with a ΔP_o power excursion, the capacitor is designed to satisfy relation (4.50) for an equivalent fictive load step $\Delta P_o'$, deduced from the power variation ΔP_o by using relation (4.58).

The proposed empirical approach is verified by simulation in Fig. 4.21 for the different values of t_{LT}, where the minimal value of the output capacitance C_o was evaluated for the operating point and circuit parameters depicted in Table 4.1.

Table 4.1 Operating point and constraints.

Nominal output voltage	$V_o = 350V$
Output voltage excursion	$\Delta v_{lim}^{(LT)} = \Delta v_{lim}^{(steady\ state)} = 2\%V_o$
Input voltage	$V_{in} = 270V$
Load power range	$P_o = [0 : 3000]W$
Switching frequency	$f_s = 20kHz$
Boost main inductance	$L = 500\mu H$
Energy controller parameters	$\omega_e = 2.5 \cdot 10^3, \zeta = 0.7, k_p = 1.76 \cdot 10^3, k_i = 1.58 \cdot 10^6$

The capacitance C_o has been evaluated for the steady state and both the load transient cases (step-up and step down), and the greatest one has been selected for the simulation:

$$C_o = \max\begin{pmatrix} C_o^{(steady\ state)} \\ C_o^{(step-down)} \\ C_o^{(step-up)} \end{pmatrix} \tag{4.59}$$

Since the output voltage constraint $\Delta v_{lim}^{(LT)} = \Delta v_{lim}^{(steady\ state)}$ has been assumed equal for the steady state and the transient behaviour, the capacitance value evaluated for the steady-state behaviour is the smallest one.

The simulation results show that the output voltage is kept within the regulation window of $\pm 0.02\ V_o$ around the nominal voltage. As expected from the C_o values obtained, the power step-up consists in the worst case, and the peak-peak undershoot amplitude is slightly larger than the overshoot one. For very smooth load transients, then for high values of t_{LT}, since the equivalent fictive load step $\Delta P_o'$ has a much lower amplitude, the C_o solutions for the load transient case tend to the steady-state C_o solution.

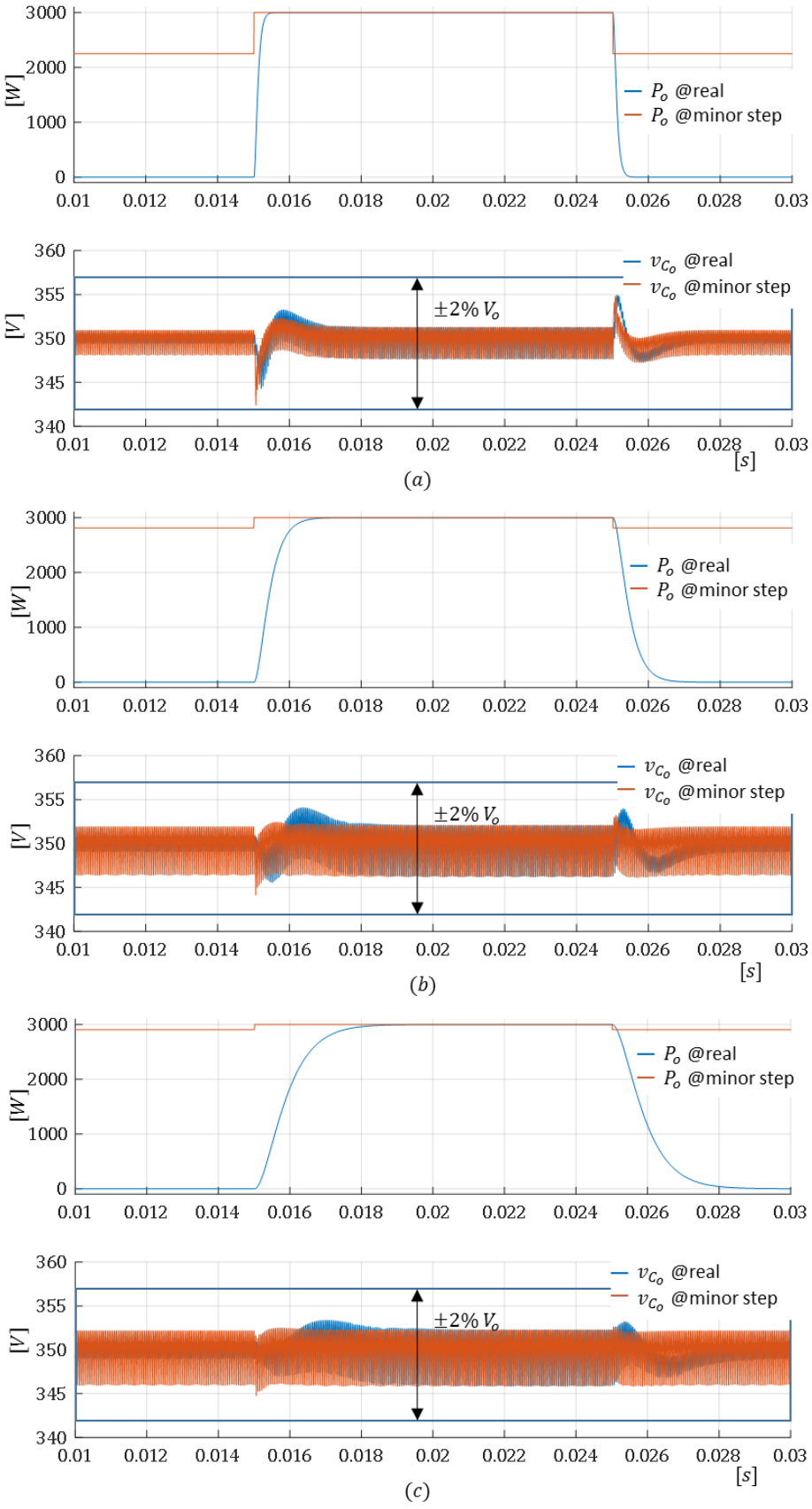


Fig. 4.21 Circuital simulation waveforms with a step-up and step-down smooth load transient with (a) $t_{LT} = 200\mu s$ ($C_o = 27.4\ \mu F, N_{LT} = 4$),(b) (a) $t_{LT} = 800\mu s$ ($C_o = 17\mu F, N_{LT} = 16$) and (c) (a) $t_{LT} = 1.6ms$ ($C_o = 22\mu F, N_{LT} = 32$).

4.6 Stability issues related to the insertion of the differential input filter

So far, the dynamic analysis conducted involved the study of the converter alone. Nevertheless, as mentioned in the previous chapter, each converter connected on the micro grid DC bus, shall meet the EMI standards defined by the builder. For the low frequency requirements, the differential noise of the input current should be kept within a specified ripple, usually by an input filter. However, the employ of an LC filter could compromise the stability of the system.

In these cases, the converters and their loads connected on the DC bus are often treated as CPLs [62], [135]. Such assumption is reasonable, especially in cases where the fast regulation of the converter (the inner regulator of the input current in the considered case) reacts at any load disturbance, making the power absorbed by the converter almost constant. Then, the system composed by the input filter and the converter, can be simplified as an LC filter in cascade with a CPL, as shown in Fig. 4.22(a), where the grid voltage is depicted as a DC voltage generator V_{in}.

The CPL voltage/current relationship is non-linear, as shown from the characteristic in Fig. 4.22(b).

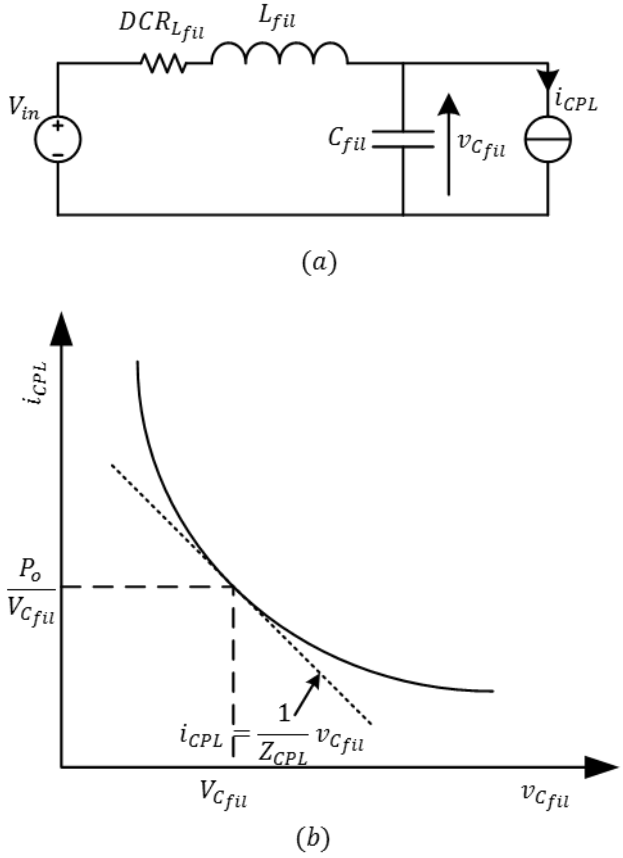


Fig. 4.22 Filter/CPL set up (a) and CPL current/voltage characteristic (b).

As showed in the system in (4.38), in order to study the dynamic behaviour in the neighbourhood of an operating point, the CPL should be linearized as follow:

$$i_{CPL} = \frac{1}{Z_{CPL}} v_{C_{fil}}, \qquad Z_{CPL} = -\frac{V_{C_{fil}}^2}{P_o} \tag{4.60}$$

Equation (4.60) describes the characteristic of the CPL curve tangent in $(i_{CPL}, v_{C_{fil}}) = (P_o/V_{C_{fil}}, V_{C_{fil}})$. The equivalent impedance of the CPL at small signal assume a negative value, which causes a voltage response in opposition to current perturbations.

At small signals, the system depicted in Fig. 4.22(a) is described by the following equations:

$$\begin{cases} L_{fil}\dfrac{d\,\tilde{\imath}_{L_{fil}}}{dt} = \tilde{v}_{in} - DCR_{L_{fil}}\,\tilde{\imath}_{L_{fil}} - \tilde{v}_{C_{fil}} \\ C_{fil}\dfrac{d\tilde{v}_{C_{fil}}}{dt} = \tilde{\imath}_{L_{fil}} + \dfrac{P_o}{V_{C_{fil}}^2}\tilde{v}_{C_{fil}} \end{cases} \tag{4.61}$$

The characteristic polynomial of the second order system in (4.61) is given by:

$$p(\lambda) = \lambda^2 + \lambda\left(\frac{DCR_{L_{fil}}}{L_{fil}} - \frac{P_o}{C_{fil}\,V_{C_{fil}}^2}\right) + \frac{1}{L_{fil}\,C_{fil}}\left(1 - \frac{P_o\,DCR_{L_{fil}}}{V_{C_{fil}}^2}\right) \tag{4.62}$$

In order to ensure that the roots of the polynomial in (4.62), which correspond to the eigenvalues of the system, have negative real parts, the polynomial coefficients should all exhibit the same sign. The stability condition is verified for the following values of P_o:

$$\begin{cases} P_o < \dfrac{DCR_{L_{fil}}}{L_{fil}} C_{fil} V_{C_{fil}}^2 \\ P_o < \dfrac{V_{C_{fil}}^2}{DCR_{L_{fil}}} \end{cases} \tag{4.63}$$

Due to the small value of DCR_{fil}, the first condition is clearly the most stringent one.

4.6.1 Stability of cascaded sub-systems

As already mentioned, the assumption of a behaviour similar to a CPL represents a perfectly controlled converter, with infinite bandwidth of the regulator. In reality, the input impedance of a real converter is more complicated than a CPL, and the interaction between an LC filter and a closed loop system needs further attention. In literature, a widely recognized method for stability analysis in the linear domain of the new system, composed of converter and its input filter, consists in the Middlebrook extra element theorem [136]. In [33], indeed, it is determined how the control-to-output transfer function G_{vd} is modified as consequence of the insertion of the input filter.

Alternatively, as in [120], [127], [137], the line-to-output transfer function can be deduced in a cascaded system composed of the input filter and the closed loop system, as shown in Fig. 4.23.

The filter and the converter are represented as quadrupoles, and it is assumed that each sub-system is stable. The relationship between current and voltage variations at the terminals can be determined through the hybrid transfer matrices:

$$\begin{bmatrix} v_{in_1}(s) \\ i_{in}(s) \end{bmatrix} = \begin{bmatrix} T_{v_{fil}}(s) & Z_{o\,fil}(s) \\ \dfrac{1}{Z_{in_{fil}}(s)} & -T_{i_{fil}}(s) \end{bmatrix} \begin{bmatrix} v_{in}(s) \\ -i_{in_1}(s) \end{bmatrix}, \tag{4.64}$$

$$\begin{bmatrix} v_o(s) \\ i_{in_1}(s) \end{bmatrix} = \begin{bmatrix} G_{vi}^{(cl)}(s) & Z_o^{(cl)}(s) \\ \dfrac{1}{Z_{in}^{(cl)}(s)} & -T_i^{(cl)}(s) \end{bmatrix} \begin{bmatrix} v_{in_1}(s) \\ i_o(s) \end{bmatrix} \tag{4.65}$$

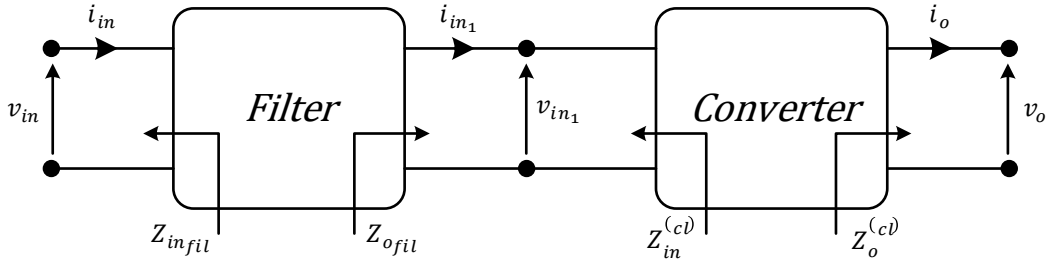


Fig. 4.23 Quadrupole equivalent scheme of the system composed of the cascade of a LC filter and a DC/DC converter.

In (4.64) and (4.65), the transfer functions are defined as:

- $T_{v_1}(s)$ and $G_{vi}^{(cl)}(s)$ are the line-to-output voltage transfer functions (voltage gain) of the input filter and the closed loop system, respectively:

$$T_{v_{fil}}(s) = \left.\frac{v_{in_1}(s)}{v_{in}(s)}\right|_{i_{in_1}(s)=0}, G_{vi}^{(cl)}(s) = \left.\frac{v_o(s)}{v_{in_1}(s)}\right|_{i_o(s)=0} \tag{4.66}$$

- $T_{i_1}(s)$ and $T_i^{(cl)}(s)$ are the output-to-line current transfer functions of the input filter and the closed loop system, respectively:

$$T_{i_{fil}}(s) = \left.\frac{i_{in}(s)}{i_{in_1}(s)}\right|_{v_{in}(s)=0}, T_i^{(cl)}(s) = \left.\frac{i_{in_1}(s)}{i_o(s)}\right|_{v_{in_1}(s)=0} \tag{4.67}$$

- $Z_{in_{fil}}(s)$ is the input impedance of the input filter, evaluated as:

$$Z_{in_{fil}}(s) = \left.\frac{v_{in}(s)}{i_{in}(s)}\right|_{i_{in_1}(s)=0} \tag{4.68}$$

- $Z_{o_{fil}}(s)$ is the output impedance of the input filter, evaluated as:

$$Z_{o_{fil}}(s) = -\left.\frac{v_{in_1}(s)}{i_{in_1}(s)}\right|_{v_{in}(s)=0} \tag{4.69}$$

- $Z_{in}^{(cl)}(s)$ is the input impedance of the converter in closed loop, evaluated as:

$$Z_{in}^{(cl)}(s) = \left.\frac{v_{in_1}(s)}{i_{in_1}(s)}\right|_{i_{in_1}(s)=0} \tag{4.70}$$

- $Z_o^{(cl)}(s)$ is the output impedance of the converter in closed loop, evaluated as:

$$Z_o^{(cl)}(s) = -\left.\frac{v_o(s)}{i_o(s)}\right|_{v_{in_1}(s)=0} \tag{4.71}$$

The study of the line-to-output transfer function of the cascaded system from (4.64) and (4.65), evaluated for a constant load current ($i_o(s) = 0$), can help for the determination of the stability:

$$v_{in_1}(s) = T_{v_{fil}}(s)v_{in}(s) - Z_{o\,fil}(s)\, i_{in_1}(s) \tag{4.72}$$

$$i_{in_1}(s)\big|_{i_o(s)=0} = \frac{v_{in_1}(s)}{Z_{in}^{(cl)}(s)} \tag{4.73}$$

$$\left.\frac{v_o(s)}{v_{in_1}(s)}\right|_{i_o(s)=0} = G_{vi}^{(cl)}(s) \tag{4.74}$$

From (4.72), (4.73) and (4.74), the line-to output transfer function is:

$$\left.\frac{v_o(s)}{v_{in}(s)}\right|_{i_o(s)=0} = \frac{G_{vi}^{(cl)}(s)\ T_{v_{fil}}(s)}{P(s)}, \tag{4.75}$$

With

$$P(s) = 1 + \chi(s), \qquad \chi(s) = \frac{Z_{o\,fil}(s)}{Z_{in}^{(cl)}(s)} \tag{4.76}$$

The functions $G_{vi}^{(cl)}(s)$ and $T_{v_{fil}}(s)$ are stable, hence only the denominator term $P(s)$ could introduce poles with negative real parts. The stability of the system can be verified by the study of the only denominator term $P(s)$. In order to avoid any kind of complications, a common way to design the input filter is indeed to ensure $Z_{o_{fil}}(s) \ll Z_{in}^{(cl)}(s)$. This condition stands for the Middlebrook criterion, which is a sufficient condition for the stability of the cascaded system. Nevertheless, for the design of the input filter, such condition could be very stringent and hard to satisfy. It could require, indeed, an excessive damping of the filter resonance, usually performed by an additional damping network composed of resistive elements (then a lower efficiency).

4.6.2 Interaction between LC input filter and Boost converter: small-signals domain analysis

In order not to overdesign the filter, a graphical approach that provides a less stringent condition can be employed.

The following analysis refers to the fourth order system shown in Fig. 4.24, composed of the boost converter and input filter state variables:

$$\begin{cases} L_{fil}\dfrac{d\tilde{\imath}_{L_{fil}}}{dt} = \tilde{v}_{in} - \tilde{v}_{C_{fil}} \\ C_{fil}\dfrac{d\tilde{v}_{C_{fil}}}{dt} = \tilde{\imath}_{L_{fil}} - \tilde{\imath}_L \\ L\dfrac{d\tilde{\imath}_L}{dt} = \tilde{v}_{C_{fil}} - (1-D)\tilde{v}_{C_o} + \tilde{d}\,V_o \\ C_o\dfrac{d\tilde{v}_{C_o}}{dt} = (1-D)\tilde{\imath}_L + \tilde{d}\,I_L + \dfrac{P_o}{V_o^2}\tilde{v}_{C_o} - \dfrac{\tilde{p}_o}{V_o} \\ \tilde{d} = F_m\left(\tilde{\imath}_{ref} - \tilde{\imath}_L - F_v\,\tilde{v}_{C_o}\right) \\ \tilde{\imath}_{ref} = C_{energy}\left(\tilde{v}_{ref} - \tilde{v}_{C_o}\right) \end{cases} \tag{4.77}$$

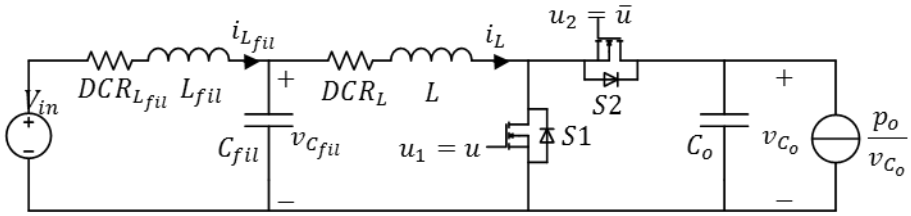


Fig. 4.24 Boost converter and LC input filter circuital scheme.

The system is controlled through the double loop controller discussed in Section 4.4 and shown in Fig. 4.25, composed of a PCM inner current controller (regulation of i_L) and an outer energy controller C_{energy} for the regulation of the electrostatic energy of C_o, defined in (4.27).

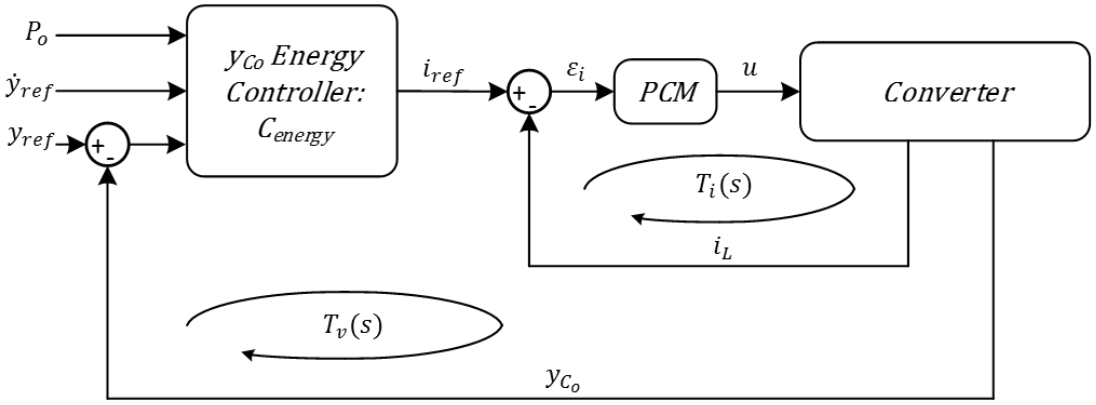


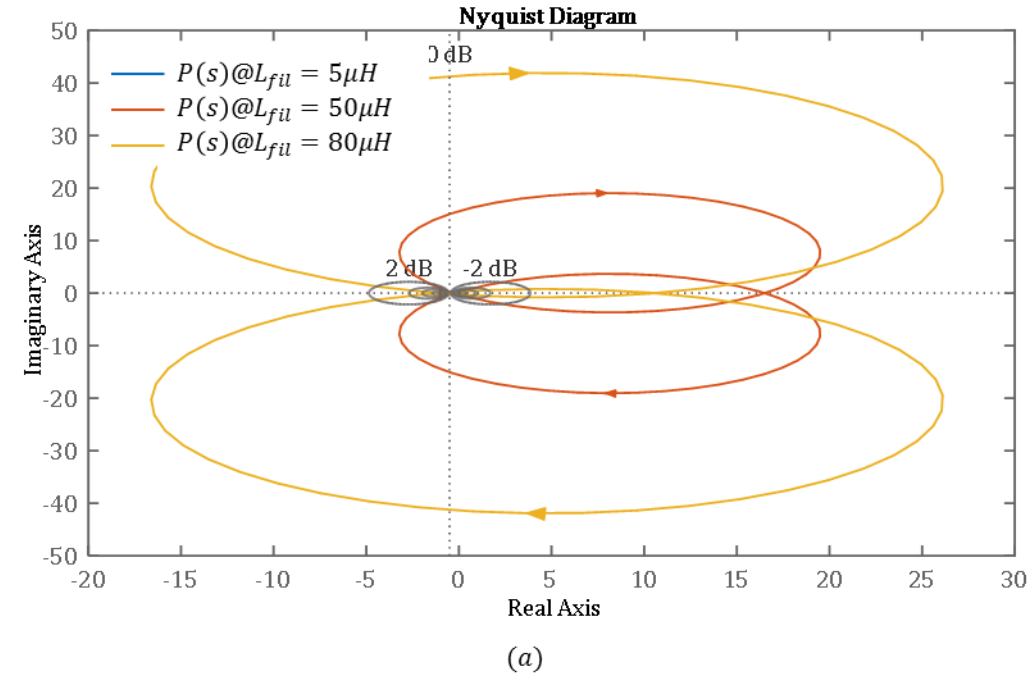
Fig. 4.25 Double loop control strategy.

The stability can be determined graphically by applying the Nyquist criterion on the term $\chi(s)$. The criterion can be verified graphically by the Nyquist plot in polar coordinates, as in Fig. 4.26. Considering the given assumptions, the system is stable if the Nyquist contour of $\chi(s)$ encircles the point (-1, 0) in the Nyquist plane in clockwise sense for a number of times equal to the number of unstable poles. In Fig. 4.26, contour map of $\chi(s)$ encircles the critical point for $L_{fil} = 80\mu H$, yet $\chi(s)$ does not exhibit unstable poles, hence the system is unstable.

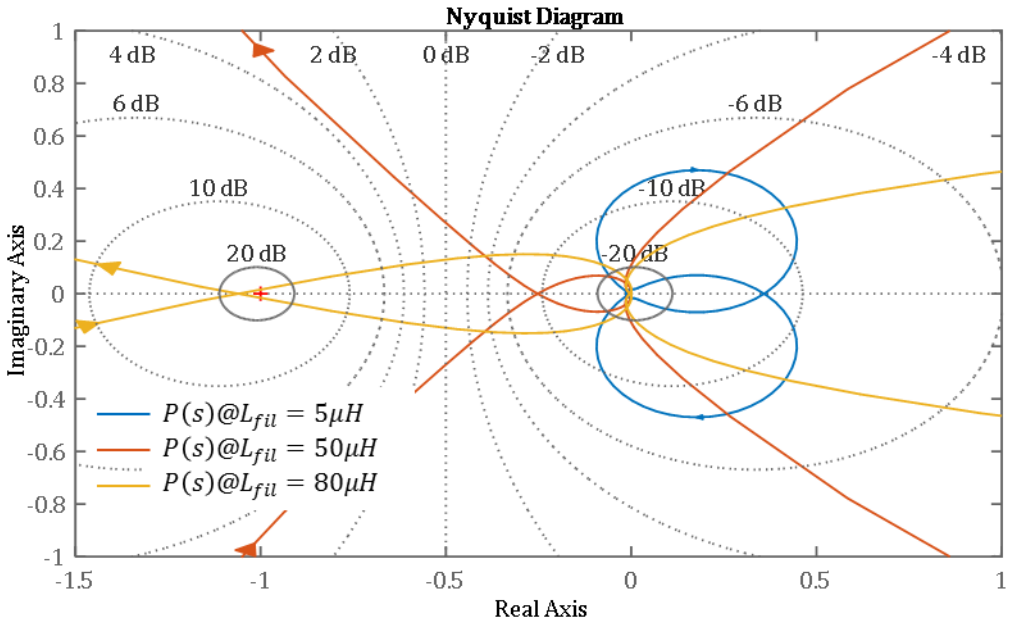
In Fig. 4.27, the value of the filter output impedance $Z_{o_{fil}}(s)$ have been modified by increasing the value of L_{fil}. Depending on the impedances ratio in Fig. 4.27, if the $Z_{o_{fil}}(s)$ resonance in ω_{fil} crosses the input impedance of the converter $Z_{in}^{(cl)}(s)$, then the Middlebrook criterion is not respected [33]. The control-to-output open loop function $G_{vd}(s)$, then the open-loop transfer functions $T_v(s)$ as well,

exhibit a glitch in the magnitude and a phase shift of 360°, as showed in Fig. 4.28 for $L_{fil} = 50\ \mu H$ and $L_{fil} = 80\ \mu H$, where $T_v(s)$ has been evaluated from the system in (4.77):

$$T_v(s) = \frac{v_{C_o}(s)}{\varepsilon_v(s)}\bigg|_{v_{in}=0, p_o=0, v_{ref}=0} \tag{4.78}$$



(a)



(b)

Fig. 4.26 Study of the Nyquist plot of $\chi(s)$ (a), zoomed around the point (-1,0) in (b), by varying L_{fil} ($V_{in} = 270V, V_o = 350V, C_o = 20\mu F, L = 500\mu H, P_o = 3000W,\ f_s = 20kHz,\ w_e = 12.5k\frac{rad}{s}, C_{fil} = 20\mu F,$ $DCR_{fil} = 0.01\ \Omega,\ L_{fil} = 5\mu H, 50\mu H, 80\mu H$).

This phenomenon could modify the gain and phase stability margins of the open loop function $T_v(s)$ and even lead to instability, as showed in Fig. 4.28 for the case $L_{fil} = 80\ \mu H$ and confirmed by the contour map in Fig. 4.26. By changing the capacitance value C_{fil}, the resonance equally moves toward smaller frequencies, but the damping factor results higher.

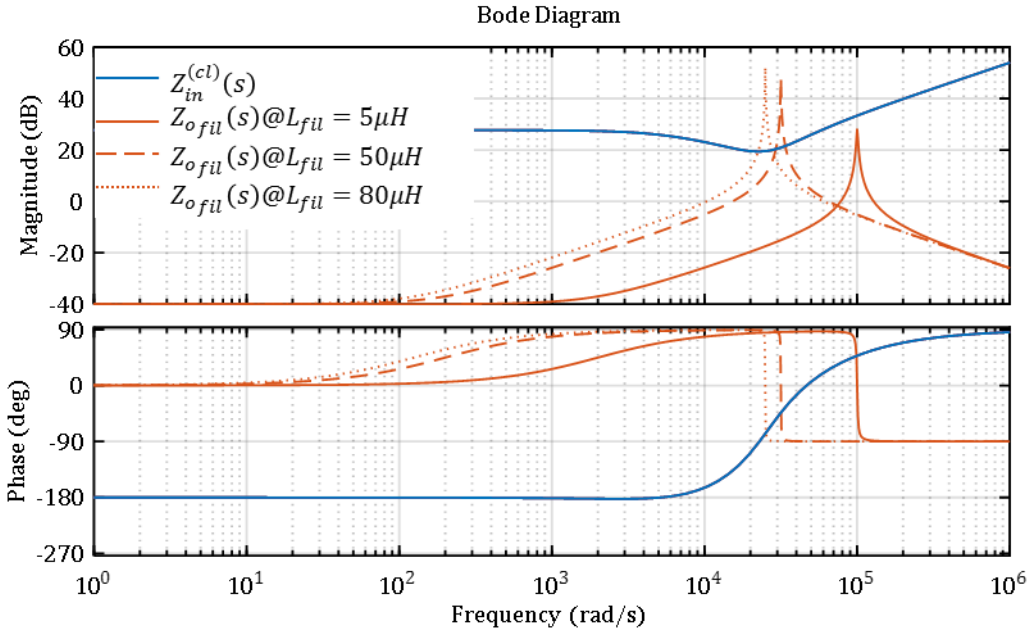


Fig. 4.27 $Z_{in}^{(cl)}(s)$ *and* $Z_{o\,fil}(s)$ *comparison by varying* L_{fil} $(V_{in} = 270V, V_o = 350V, C_o = 20\mu F, L = 500\mu H, P_o = 3000W,\ f_s = 20kHz,\ w_e = 12.5k\frac{rad}{s}, C_{fil} = 20\mu F,\ DCR_{fil} = 0.01\ \Omega,\ L_{fil} = 5\mu H, 50\mu H, 80\mu H)$.

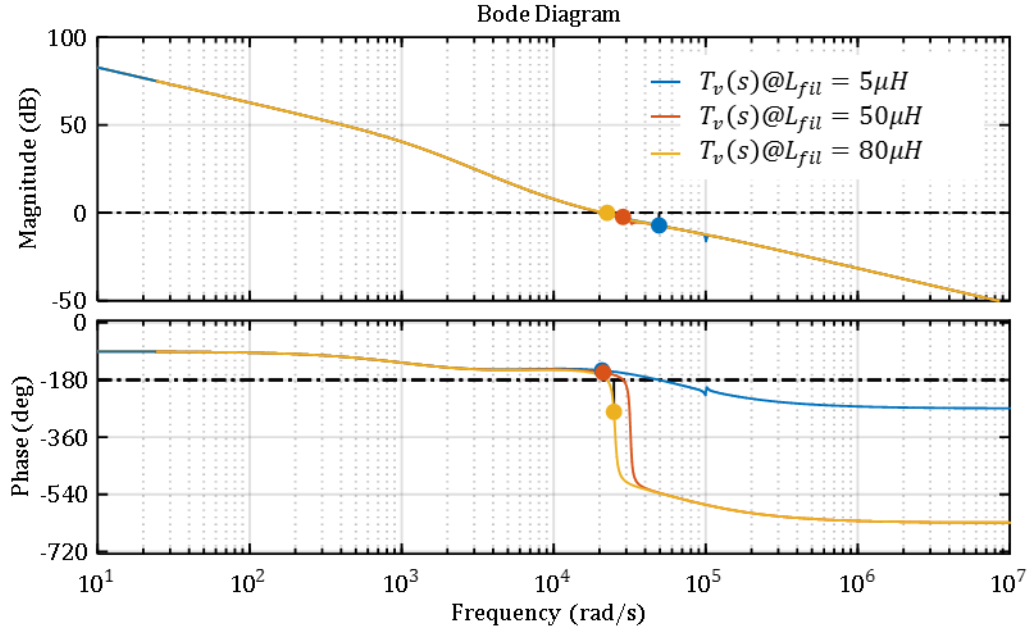


Fig. 4.28 Boost+filter control-to-output $G_{vd}(s)$ *and open loop compensated transfer function* $T_v(s)$ *comparison by varying* $L_{fil}(V_{in} = 270V, V_o = 350V, C_o = 20\mu F, L = 500\mu H, P_o = 3000W,\ f_s = 20kHz,\ w_e = 12.5k\frac{rad}{s}, C_{fil} = 20\mu F,\ DCR_{fil} = 0.01\ \Omega,\ L_{fil} = 5\mu H, 50\mu H, 80\mu H)$.

For resonance values ω_{fil} larger than the crossover frequency of the outer loop open loop function, if $Z_{o_{fil}}(s)$ is poorly damped, it could cause undesirable effects, such as multiple crossing at 0dB.

However, the aim of the thesis work is to develop a tool for the verification of the stability that could be included in an optimization algorithm. It is clear that the graphical approaches do not fit well with such intent. With a more consistent computational effort, the evaluation of the eigenvalues of the cascaded system could be included in the routine of an optimization algorithm. Moreover, it should be reminded that, for frequencies two decades below the switching one, such considerations are no longer valid.

4.6.3 Interaction between LC input filter and Boost converter: discrete time domain analysis

Alternatively, the system can be mapped in the discrete time, with a T_s sampling time, in order to obtain a model reliable for the whole range of frequencies up to the switching one. The study of the eigenvalues of the controlled system Jacobian matrix can be employed to verify the stability. In [124], the same analysis has been conducted for a third order system. In the following section, the discrete mapping has been performed for a fifth order system.

As showed in [138], if the state variables equations systems are integrable over the respective sequence relative to the specific circuit configuration, it is possible to obtain a relationship which relates the state variable vector at the time $(n+1)T_s$ and the one at nT_s. For the considered system, two sequences and a scalar input variable d are considered:

$$\boldsymbol{x}[(n+1)T_s\,] \;= \boldsymbol{f}[\boldsymbol{x}(n\,T_s\,), d(n\,T_s)] \tag{4.79}$$

Where $\boldsymbol{x}$ is the state variable vector defined as:

$$\boldsymbol{x} = \begin{bmatrix} i_L \\ i_{L_{fil}} \\ v_{C_{fil}} \\ v_{C_o} \end{bmatrix} \tag{4.80}$$

The system can be expressed in each sequence through the state space matrix form:

$$\dot{\boldsymbol{x}} = A_i \boldsymbol{x} + B_i \;, i = 1{,}2 \tag{4.81}$$

The A_i and B_i dynamical matrices are from the circuital analysis of the system in Fig. 4.24 in the two sequences ($i = 1$ for when $u_1 = 1$ and $u_2 = 0$, $i = 2$ in the reverse case):

$$A_1 = \begin{bmatrix} -\dfrac{DCR_L}{L} & 0 & \dfrac{1}{L} & 0 \\ 0 & -\dfrac{DCR_{L_{fil}}}{L_{fil}} & -\dfrac{1}{L_{fil}} & 0 \\ -\dfrac{1}{C_{fil}} & \dfrac{1}{C_{fil}} & 0 & 0 \\ 0 & 0 & 0 & \dfrac{P_o}{C_o V_o^2} \end{bmatrix}, \tag{4.82}$$

$$A_2 = \begin{bmatrix} -\frac{DCR_L}{L} & 0 & \frac{1}{L} & -\frac{1}{L} \\ 0 & -\frac{DCR_{L_{fil}}}{L_{fil}} & -\frac{1}{L_{fil}} & 0 \\ -\frac{1}{C_{fil}} & \frac{1}{C_{fil}} & 0 & 0 \\ \frac{1}{C_o} & 0 & 0 & \frac{P_o}{C_o V_o^2} \end{bmatrix} \tag{4.83}$$

$$B_1 = B_2 = \begin{bmatrix} 0 \\ \frac{V_{in}}{L_{fil}} \\ 0 \\ -2\frac{P_o}{C_o V_o} \end{bmatrix} \tag{4.84}$$

In order to allow a linear resolution, the current of the CPL has been linearized around the nominal load power P_o.

The solution in the time domain of a linear non-homogeneous equations system with constant dynamic matrix A_i, as the one in (4.82) and (4.83), is given by:

$$\boldsymbol{x}(t) = e^{A_i\,(t-t_0)}\,\boldsymbol{x}(t_0) + \int_{t_0}^{t} e^{A_i\,(t-\tau)} B_i\,d\tau \tag{4.85}$$

Assuming the input value $d(n)$ is known, the value of the state variables at $t = (n + d(n))T_s$ is given by:

$$\begin{aligned} \boldsymbol{x}\big((n+d(n))T_s\big) &= e^{A_1\,d(n)T_s}\,\boldsymbol{x}(n\,T_s) + \int_0^{d(n)T_s} e^{A_1\,(d(n)T_s-\tau)} B_1\,d\tau \\ &= e^{A_1\,d(n)T_s}\,\boldsymbol{x}(n\,T_s) + \big(e^{A_1\,d(n)T_s} - \mathbb{I}\big)A_1^{-1}B_1 \end{aligned} \tag{4.86}$$

Where $\mathbb{I}$ represents the identity matrix of the fourth order.

The value obtained in (4.86) can be used as the initial point of the differential equation in (4.85) for the resolution of the second sequence:

$$\begin{aligned} \boldsymbol{x}\big((n+1)T_s\big) &= e^{A_2\,(1-d(n))T_s}\,\boldsymbol{x}\Big(\big(n+d(n)\big)T_s\Big) + \int_0^{(1-d(n))T_s} e^{A_2\,\left((1-d(n))T_s-\tau\right)} B_1\,d\tau \\ &= e^{A_2\,(1-d(n))T_s}\,\boldsymbol{x}\Big(\big(n+d(n)\big)T_s\Big) + \big(e^{A_2\,(1-d(n))T_s} - \mathbb{I}\big)A_2^{-1}B_2 \\ &= e^{A_2\,(1-d(n))T_s}\big(e^{A_1\,d(n)T_s}\,\boldsymbol{x}(n\,T_s) + \big(e^{A_1\,d(n)T_s} - \mathbb{I}\big)A_1^{-1}B_1\big) \\ &+ \big(e^{A_2\,(1-d(n))T_s} - \mathbb{I}\big)A_2^{-1}B_2 \end{aligned} \tag{4.87}$$

Equation (4.87) provides a discrete map of the system with sampling time T_s.

In order to check the validity of the evaluated discrete model in (4.87), it has been compared in MATLAB Simulink simulation of the controlled converter, through the Power Sim tool. The simulation results are shown in Fig. 4.29, in steady state and step-down load transient conditions.

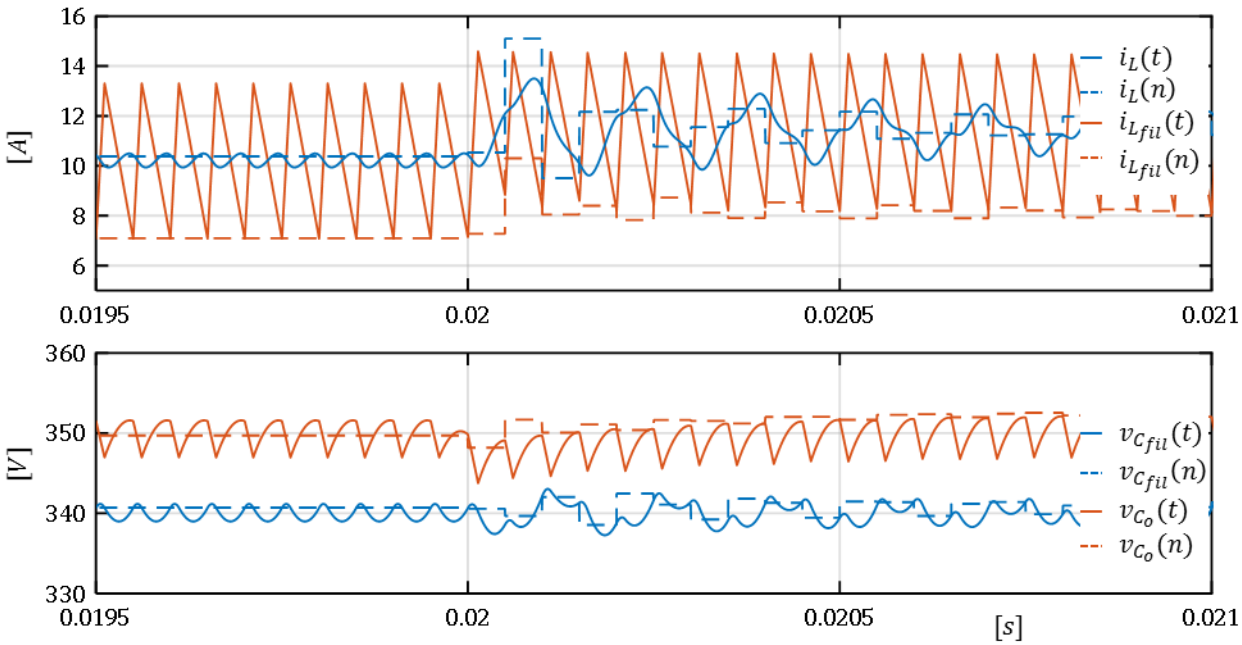


Fig. 4.29 Comparison between real elements simulation and discrete model ($V_{in} = 270V, V_o = 350V, C_o = 20\mu F, L = 500\mu H, \Delta P_o = 3000W,\ f_s = 20kHz,\ \omega_e = 2.5k\frac{rad}{s}, C_{fil} = 20\mu F,\ L_{fil} = 30\mu H$).

The dashed lines represent the sampled system obtained through (4.87). It can be remarked that the discrete state variables values match with the continuous ones at the beginning of each switching period. The simulation and the discrete values are consistent even during the load transient. However, when the output power is not at its nominal value P_o, the output voltage $v_{C_o}(n)$ exhibits a small deviation from the simulation values $v_{C_o}(t)$, due to the linearization error of the CPL current.

The validation of the stability should be now conducted on the closed loop system. The control strategy is the one introduced in Section 4.4 (Fig. 4.25). The control law of the outer loop involves the integral term of the energy error $\varepsilon_{y_{C_o}}$. In order to address an integral term in the control law, the system should be extended and another variable Γ is included:

$$\Gamma = \frac{1}{2} C_o \int V_o^2 - v_{C_o}^2(t)\, dt, \tag{4.88}$$

Because of the $v_{C_o}^2$ term, the state equation relative to the time variation of Γ is not linear:

$$\dot{\Gamma} = \frac{1}{2} C_o \left(V_o^2 - v_{C_o}^2(t) \right) \tag{4.89}$$

Furthermore, even if one could think to linearize (4.89), the dynamic matrices of the extended will be singular, as shown for the example on the first sequence dynamic matrix:

$$\boldsymbol{x}=\begin{bmatrix} i_L \\ i_{L_{fil}} \\ v_{C_{fil}} \\ v_{C_o} \\ \Gamma \end{bmatrix},\quad A_1=\begin{bmatrix} -\frac{DCR_L}{L} & 0 & \frac{1}{L} & 0 & 0 \\ 0 & -\frac{DCR_{L_{fil}}}{L_{fil}} & -\frac{1}{L_{fil}} & 0 & 0 \\ -\frac{1}{C_{fil}} & \frac{1}{C_{fil}} & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{P_o}{C_o V_o^2} & 0 \\ 0 & 0 & 0 & -C_o V_o & 0 \end{bmatrix} \tag{4.90}$$

Matrices A_1 and A_2 appear inverted in (4.87), so it is necessary that they are not singular.

For these two reasons, the discrete relation between Γ at the time $t = nT_s$ and at $t = (n+1)T_s$ has been evaluated analytically by (4.88) and the time function of v_{C_o} evaluated in (4.87).

The system, as obtained in (4.87), still shows a dependency from the input value $d(n)$. In order to analyse the system in closed loop, the input value shall be expressed through the control law as function of the state variables. The switching surface, which determines the commutation time $t = \big(n + d(n)\big)T_s$ between the two sequences, can be expressed as:

$$s(t) = i_{ref}(t) - i_L(t) + m_c\left(\frac{T_s}{2} - t\right), \qquad s(dT_s) = 0 \tag{4.91}$$

In (4.91), the duty cycle $d(n)$ appears in the $i_L(t)$ term and in the reference current law $i_{ref}(t)$ through the output voltage $v_{C_o}(t)$ (Equation (4.37)). The time functions of $i_L(t)$ and $v_{C_o}(t)$ are evaluated through the fourth order system in (4.87). Nonetheless, the dependence of the switching surface $s(t)$ in (4.91) from the duty value d is not explicit.

However, (4.91) can be used to evaluate an explicit formulation of the Jacobian matrix of the controlled system in the neighbourhood of the operating point.

The duty cycle value d must verify the relation $s(dT_s) = 0$, then, from the implicit equation in (4.91), the first term of the Taylor expansion can be deduced:

$$\sum_{i=1}^{N} \frac{\partial s}{\partial x_i}\delta x_i + \frac{\partial s}{\partial d}\delta d = 0 \tag{4.92}$$

Where $\boldsymbol{x} = \left[i_L, i_{L_{fil}}, v_{C_{fil}}, v_{C_o}, \Gamma\right]$ is the extended state variables vector, $\boldsymbol{f}$ is the array system function of the same order and $N = 5$ is the order of the system:

$$\boldsymbol{x}[(n+1)T_s\,] \;= \boldsymbol{f}[\boldsymbol{x}(n\,T_s\,), d(n\,T_s)] \tag{4.93}$$

The infinitesimal increment of d is then:

$$\delta d = -\left(\frac{\partial s}{\partial d}\right)^{-1} \sum_{i=1}^{N} \frac{\partial s}{\partial x_i}\delta x_i \tag{4.94}$$

In the same way, the first term of the Taylor expansion of the system in (4.91) in the neighbourhood of the operating point is expressed as:

$$\delta \boldsymbol{f} = \begin{bmatrix} \sum_{i=1}^{N} \frac{\partial f_1}{\partial x_i} \delta x_i + \frac{\partial f_1}{\partial d} \delta d \\ \vdots \\ \sum_{i=1}^{N} \frac{\partial f_m}{\partial x_i} \delta x_i + \frac{\partial f_m}{\partial d} \delta d \\ \vdots \\ \sum_{i=1}^{N} \frac{\partial f_N}{\partial x_i} \delta x_i + \frac{\partial f_N}{\partial d} \delta d \end{bmatrix} \tag{4.95}$$

From (4.95) and (4.94), the $\boldsymbol{f}$ function increment becomes:

$$\delta \boldsymbol{f} = \begin{bmatrix} \sum_{i=1}^{N} \frac{\partial f_1}{\partial x_i} \delta x_i - \frac{\partial f_1}{\partial d} \left(\frac{\partial s}{\partial d}\right)^{-1} \frac{\partial s}{\partial x_i} \delta x_i \\ \vdots \\ \sum_{i=1}^{N} \frac{\partial f_m}{\partial x_i} \delta x_i - \frac{\partial f_m}{\partial d} \left(\frac{\partial s}{\partial d}\right)^{-1} \frac{\partial s}{\partial x_i} \delta x_i \\ \vdots \\ \sum_{i=1}^{N} \frac{\partial f_N}{\partial x_i} \delta x_i - \frac{\partial f_N}{\partial d} \left(\frac{\partial s}{\partial d}\right)^{-1} \frac{\partial s}{\partial x_i} \delta x_i \end{bmatrix} \tag{4.96}$$

It is finally possible to evaluate the Jacobian matrix $\mathbb{J}$ of the system in (4.96) in the local neighbourhood of the operating point:

$$\mathbb{J} = \begin{bmatrix} \frac{\partial f_1}{\partial x_1} \delta x_i - \frac{\partial f_1}{\partial d} \left(\frac{\partial s}{\partial d}\right)^{-1} \frac{\partial s}{\partial x_1} \delta x_1 & \cdots & \frac{\partial f_1}{\partial x_N} \delta x_N - \frac{\partial f_1}{\partial d} \left(\frac{\partial s}{\partial d}\right)^{-1} \frac{\partial s}{\partial x_N} \delta x_N \\ \vdots & \ddots & \vdots \\ \frac{\partial f_N}{\partial x_1} \delta x_i - \frac{\partial f_N}{\partial d} \left(\frac{\partial s}{\partial d}\right)^{-1} \frac{\partial s}{\partial x_1} \delta x_1 & \cdots & \frac{\partial f_N}{\partial x_N} \delta x_N - \frac{\partial f_N}{\partial d} \left(\frac{\partial s}{\partial d}\right)^{-1} \frac{\partial s}{\partial x_N} \delta x_N \end{bmatrix} \tag{4.97}$$

The eigenvalues λ_i of the matrix $\mathbb{J}$ are the solutions of the equation below:

$$|\mathbb{J} - \lambda \, \mathbb{I}| = 0 \tag{4.98}$$

With $\mathbb{I}$ the identity matrix of the N^{th} order. The stability condition for a discrete system is verified if $|\lambda_i| < 1$.

4.7 Conclusions

In this chapter, the dynamic behaviour of the DC/DC converter has been discussed. It has been shown that, for a motor drive application, the actuator composed by the VSI and the PMSM could exhibit a fast variation of the required power, due to the performant controller of the inverter phases currents. The power variation of the converter load could cause some dangerous excursion of the output voltage, which could compromise the controllability of the inverter phase currents.

The dynamical analysis has been conducted for a DC/DC boost converter, and the system has been characterized by means of small signals modelling. The frequency analysis of the converter transfer functions showed dynamical limitations due to the right half plane zero, common in all the boost-derived topologies. Such issue is a restraining factor for the control strategy of the converter. It has been showed that the choice of a single loop control strategy is unsuitable for the range of power and circuit parameters values (switching frequency, capacitance and inductance values) usually considered for such applications. A double loop strategy is in fact the most common choice, which also allows to control the inductor current and contain its variation. As for the inner current loop, a peak current controller has been chosen because of its robustness, rapidity and large employ in these kinds of applications.

Since the main task is to contain the output voltage variation during a possible variation of the output power, a control strategy featured by a better rejection of the output load disturbances has been proposed: if the controller ensures a good immunity from the load disturbances, the output capacitor must not be oversized to contain the excursion of the output voltage. In this regard, an analytical way to design the output capacitor has been proposed in order to keep the output voltage undershot/overshot of the controlled system during load power transients within the assumed voltage constraints. The minimal value of capacitance obtained will depend on the operating point parameters, the switching frequency, the inductance value and the controller parameters as well.

In the last section, the stability issue is discussed. Due to the high dynamic performance of the converter input current, the dynamic behaviour of the actuator assembly can be considered as a negative impedance, which could lead toward instability issues. The interaction between the closed loop system and the input filter has been analysed in the linear domain in a first approach, specifically by analysing the input impedance of the closed loop system and the output impedance of the filter affects the poles of the global system. Such method, even if largely used, is unable to include the non-linear effects due to the switching behaviour of the real system. For this reason, a more reliable tool has been developed to analyse the stability of the system even for frequencies close to the switching one. The approach consists of a discrete mapping of the system in steady state to deduce its dynamical (Jacobian) matrix. The time evolution of the discrete system is consistent with the one of the continuous time system in simulation, which proves the reliability of the obtained system. The analysis of the matrix eigenvalues allow to verify the stability of the system composed by the LC input filter, the DC/DC converter and a constant power load. This tool is more likely suitable to be included in an optimization routine, as discussed in Chapter 5.

5 Multi-Objective Optimization of a DC/DC Boost Converter

5.1 Introduction: Optimization Problem

As illustrated in the previous chapters, the design of a DC/DC converter is a complex task. The choice and the design of each element involve several parameters. Knowledge and experience lead the designer to obtain the desirable features and performances, all this by complying with the specifications set provided for the specific application, the feasibility constraint related to the technology and availability on the market and the safety margin accounted to ensure a reasonable reliability of the component during the normal operation. Furthermore, as highlighted in the manuscript, the choice of each element of the converter should be conducted taking into account the impact it has on the choice of the other elements of the converter and on the overall required performances of the converter itself (stability, efficiency, reliability, cost etc.).

Currently, several design approaches consist of step-by-step procedures or guidelines [97], [139]. A possible routine could be composed of the following major steps:

- Depending on the nature of the application and on the respective requirements, a converter topology and the design goals are chosen;
- Technology and material of the converter elements are chosen depending on the costs and the commercial availability;
- The maximal ratings and the desired performances of each element of the power stage are assigned depending on both operating point and the designer experience, as for example the switch current ratings, the amount of power losses assigned to each component or the size goals of the magnetics;
- The operating switching frequency is often chosen accordingly to the thermal capability of the semiconductor switching devices chosen, their technology and the cooling system;
- By following the considered constraints and the self-imposed guidelines, the design of each element of the converter is conducted. Besides, even the parameter choices of the converter element alone may imply several trade-offs, as, for example, for the design of the magnetic elements.

In order to reduce the large variety of coupled parameters to choose and the degrees of freedom of such kind of problems, the designer is forced to isolate the design of the individual elements, to impose design constraints and to make arbitrary assumptions and trade-off decisions. For these reasons, a considerable amount of the efforts focuses on optimizing specific components or subsystems of the converter [95], [140]. All the assumptions made may prevent from exploring the whole design space of such parameters and to possibly obtain more performant design solutions, especially when the problem requires the optimization of more than one feature or performance. Indeed, when the design goals are manifold, the objectives could be in competition, and the design decisions must arrange a trade-off between the desired performances.

Moreover, so far, the dynamical considerations can be accounted only in an approximated and qualitative way during the design procedure. Any impact on the dynamic features of the converter, resulting from the choice of the power circuit elements, can only be observed after the choice of the control strategy. According to the transitory requirements and the possible disturbances expected in the course of the operating profile of the application, the designer can subsequently choose the most

convenient control strategy. As showed in Chapter 4, in order to meet the control-dependent performance requirements such as stability, responses to line/load transients, or other disturbances, the design of the control circuit for a given power circuit cannot disregard the elements of the converter power stage and its dynamical characteristics (described by the open loop transfer functions), because the practical limitations and the non-ideality of the controller (duty-cycle, limited bandwidth).

It is clear that such an approach cannot guarantee the optimality of the obtained design solution in regards to more conflicting performances and targeted features. A step-by-step procedure, based on arbitrary choices and decision of the designer, is clearly unable to solve a multi-objective problem as the design of a power converter.

Due to the large searching space, composed of the admissible ranges of the design variables, in most cases it is impossible to find a unique optimal solution which satisfies all the required performances in the best possible way. In a multi-objective optimization problem, multiple objective performances coexist and shall be satisfied. The simultaneous optimization of all the conflicting objectives is clearly not possible. The design solutions shall represent the best solutions among the whole set of possible trade-offs. Each optimal solution, also called Pareto optimal solution [141], or non-dominated solution, can be considered as such when none of the global objective performances can be improved in value without degrading some of the others.

Furthermore, as already discussed, the selection of the design variables shall respect several constraints, such as feasibility, ratings of the components and application specifications. Usually, the constraints criteria which determine the eligibility of a solution composed by a given set of variables consist in non-linear relationships.

In this context, mathematical optimization tools offered new methodical design approaches, ways to employ less simplifications and to deal with more design variables, helped by development of the increasing computational power of the calculators. Among the existing methods, two great families of tools can be distinguished: deterministic and stochastic algorithms.

In deterministic algorithms, the convergence toward optimal solutions is conducted by fixed mechanisms, which, for the same inputs, lead always to the same results. Nevertheless, many practical engineering problems involve multi-modal and non-differentiable nonlinear functions of several design variables, which are pretty challenging to handle with deterministic algorithms [142].

For the aforementioned reasons, stochastic algorithms have been far more successful in literature [142], [143], due to their simplicity. Unlike the deterministic algorithms, they are based on random mechanisms for the research of the global optimum solutions. They are usually based on metaheuristic processes, which employ nature inspired dynamics. Among them, evolutionary algorithms have received a great interest in the recent years, namely the genetic algorithms [144]–[146].

In this context, one of the most efficient genetic algorithms is surely the *non-dominated sorting genetic algorithm* (NSGA-II) [147]. This method has been applied to find the most convenient design solutions for a constrained multi-objective optimization problem of a DC/DC converter for a motor drive application, as described in the previous chapters.

In this chapter, a brief review on the structure of a multi-objective optimization problem is discussed, specifically framed for a power converter design. After a first introduction, where the common desired features of a converter are described, the optimization problem is presented in a formal way. The design optimization problem of the DC/DC boost converter is formalized: the design variables and parameters, the objective functions relative to the volume and the power losses, and the constraints functions which verify the feasibility of each solution. The NSGA II routine is analysed and performed for the considered problem. Eventually, in order to prove the validity of the design approach, a design solution has been selected to build a boost converter prototype and implemented on a test-bench.

5.1.1 Figure of Merits

In order to properly evaluate the performances of a converter, performance metrics need to be defined. Depending on the requirements, the objective functions (cost functions) represent the goals of the multi-objective optimization.

In literature, several figures of merits (FOM, [145], [148], [149]) help the designers comparing the performances of power electronics converters over a wide power range and different applications. For this reason, these functions are usually normalized, so to characterize a system independently from the electrical nominal values.

In the following list, the definitions of the most common FOM are summarized in their normalized form:

- *Power density:* the output power density characterizes the degree of compactness of a converter or the volume required for realization at a given rated power. It is defined as:

$$\rho = \frac{P_o}{V_{(converter)}} \tag{5.1}$$

  In (5.1), P_o is the converted power and V_{tot} is the overall volume. In an application where the supplied output power may vary, the P_o value employed in (5.1) should correspond to the maximum one. The major contribution to the volume of the converter comes from the inductive and capacitive components and the cooling system. If the calculation of the converter volume is the sum of each individual component volume, the whole packaging must be accounted. Higher values of power density can be achieved by adapting the component shapes or by multi-functional use of some components (for example the use of the same magnetic core for the common mode and the differential mode rejection, or by using a magnetic core for the dissipation of heat).

- *Efficiency:* Consequently, to the rising of the energy prices and the environmental issues, the high efficiency of the power electronics systems becomes a requirement of primary importance. It is defined as:

$$\eta = \frac{P_o}{P_{in}} = \frac{P_o}{P_o + P_{(converter)}} \tag{5.2}$$

  Where P_{in} is the input power in a specific operating point and $P_{(converter)}$ stands for the system losses. The efficiency value alone is not a sufficient information. Indeed, the efficiency changes along with the operative conditions, such as load power and nominal voltages. Often, a power system which works at partial load shows a lower efficiency, hence its value should be specified along with the operating point at which it has been evaluated. For systems designed to work over wide input and/or output voltage ranges, a high efficiency is difficult to attain. In case of such applications, where the operating points changes, it is more reasonable to define a mean mission efficiency:

$$\eta = \frac{1}{1 + \frac{\int_0^{T_m} P_o \, dt}{\int_0^{T_m} P_{(converter)} \, dt}} \tag{5.3}$$

  The mission efficiency, however, can only be defined by knowing the mission profile of the output load power. Indeed, the comparison with a system designed for a specified operating point would not be fair or have any meaning.

- *Output power per unit weight:* even if it is hardly treated in literature, this figure of merit can be even more interesting than the power density:

$$\gamma = \frac{P_o}{M_{(converter)}} \tag{5.4}$$

  Especially for mobile applications, the weight of the conversion chain determine directly the fuel consumption.
- *Relative costs:* the power that can be converted for a given cost $C_{(converter)}$ represents an extremely influent factor, especially in industrial applications:

$$\sigma = \frac{P_o}{C_{(converter)}} \tag{5.5}$$

  This parameter need to be contextualized in each case. The costs for realization of a system, however, depend on the number of elements of the converter, hence the topology and the employed technology. Moreover, it is a challenging task to provide a reliable model of the cost of the electronic components. Indeed, besides the effective cost of production, the price is influenced by several economic related factors. A reliable calculation of the relative costs is hence only possible if cost models are available, and it is clear that the realization of a model need a considerable amount of data concerning the market prices of the components. The collection of such data is often impeded by sellers and manufacturers because of their non-disclosure policy.
- Reliability: The reliability of a converter (or of a single component) is defined as the ability to perform its task at given conditions for a given period of time, which is a fundamental requirement in certain applications (aerospace or space applications). The characterization of the reliability is not frequently considered, since it is a challenging feature to estimate: before the realization of a prediction model, a large amount of experimental test needs to be conducted, which can last even for years. An important and widely used reliability index is the mean time between failure (MTBF) or mean time to failure (MTTF)[150]:

$$MTBF = \frac{1}{\sum_{i=1}^{N_\gamma} \gamma_i} \tag{5.6}$$

  where γ_i is used to indicate the i^{th} converter component failure rate per time unit, and N_γ is the number of components in the converter.

As for the case under study, the efficiency of the converter and its power density have been considered as primary criteria, since autonomy and compactness are strongly required for embedded applications. However, the optimisation could be adapted to carry out more tasks, without compromising the originality of the work, the main purpose of which was to develop a method for including the transient behaviour of the converter in an optimal multi-objective design.

5.1.2 Optimization problem: Design Variables Space and Performance Space

In this section, the proper formulation of a constrained multi-objective optimization problem is addressed. In mathematical terms, given a n-dimensional array which represents the design

parameters/variables set, it belongs to a limited design variables space Ω, called feasible design space, defined as:

$$\boldsymbol{x} \in \mathbb{R}^n, \tag{5.7}$$

$$\boldsymbol{h}_i: \mathbb{R}^n \to \mathbb{R}^l, \qquad \boldsymbol{h}_e: \mathbb{R}^n \to \mathbb{R}^g \tag{5.8}$$

$$\Omega = \{\boldsymbol{x} \in \mathbb{R}^n \mid \boldsymbol{h}_i(\boldsymbol{x}) \leq 0 \cap \boldsymbol{h}_e(\boldsymbol{x}) = 0\} \tag{5.9}$$

With $\boldsymbol{h}_i(\boldsymbol{x})$ and $\boldsymbol{h}_e(\boldsymbol{x})$ being the constraint vector functions, respectively composed by l and g constraint functions, which define the feasibility of the solutions $\boldsymbol{x}$, hence the domain Ω. The constraints can indeed be expressed as equalities or inequalities conditions, as in (5.9), which correspond to the analytical formulations of the application specifications (operating point) or feasibility limitations, such as maximal temperature, maximal ratings and magnetic saturation.

Once the required m goals are expressed through proper analytical models, for each solution $\boldsymbol{x}$, an image $\boldsymbol{y}$ can be mapped in the Λ performance space through the vector of the objective functions $\boldsymbol{F}(\boldsymbol{x})$:

$$\boldsymbol{F}: \mathbb{R}^n \to \mathbb{R}^m, \tag{5.10}$$

$$\Lambda = \{\boldsymbol{y} \in \mathbb{R}^m \mid \boldsymbol{y} = \boldsymbol{F}(\boldsymbol{x}), \quad \boldsymbol{x} \in \Omega\} \tag{5.11}$$

A bi-dimensional example of the domains Λ and Ω is depicted in Fig. 5.1.

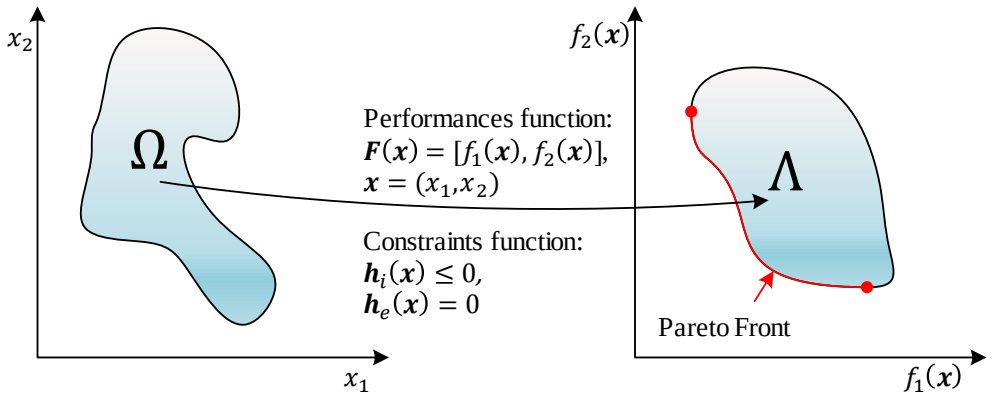


Fig. 5.1 Bi-dimensional example of design space and performance space domains.

In an optimization problem, the designer would aim to find the $\boldsymbol{x}$ solutions set which corresponds to the best compromise between all the cost function values. In a non-trivial multi-objective optimization problem it does not exist a unique solution vector, which simultaneously minimizes (maximizes, for maximization problems) each objective function, i.e. the performance functions are conflicting. Then, the concept of Pareto optimality is usually applied [141], [149], [151]. The research of a set of Pareto optimal solutions correspond to individuate the set of solutions $\boldsymbol{x}$ whose images $\boldsymbol{y}$ are non-dominated (non-inferior). Given an objective vector function:

$$\boldsymbol{F}(\boldsymbol{x}) = [f_1(\boldsymbol{x}), f_2(\boldsymbol{x}) \dots f_m(\boldsymbol{x})] \tag{5.12}$$

In a minimization problem, where the task consists of finding the $\boldsymbol{y}$ values closer to the origin, a non-dominated solution $\boldsymbol{x}^*$ should satisfy the following conditions:

$$f_i(\boldsymbol{x}^* + \Delta\boldsymbol{x}) \leq f_i(\boldsymbol{x}), \qquad i \in [1,\ldots,m],\ (\boldsymbol{x}^* + \Delta\boldsymbol{x}) \in \Omega, \tag{5.13}$$

$$\exists j \in [1,\ldots,m] \ \mid f_j(\boldsymbol{x}^* + \Delta\boldsymbol{x}) < f_j(\boldsymbol{x}). \tag{5.14}$$

In other terms, in an indefinitely large neighbourhood of the non-dominated solution $\boldsymbol{x}^*$, there is no other solution vector whose all the objective functions exhibit smaller values (larger, in a maximization problem).

Graphically, as indicated in Fig. 5.1, the images of the set of Pareto solutions lie on the left-inferior border.

5.1.3 Genetic Algorithms: NSGA II

Stochastic evolutionary algorithms, like the genetic ones, are based on Darwin 's evolution theory. The evolution and the survival of the breeding (population) individuals, identified by a string of genes, is handled by natural selection phenomena, like reproduction and mutation.

In a genetic algorithm, a population of individuals simulates the breeding environment, where each individual refers to a design solution, also called *genome*. The algorithm flowchart is showed in Fig. 5.2.

The main steps may be summed up as follows:

- *Starting Population*: Once the design variables, hence the genome, the constraint functions and the objective functions are defined, the procedure begins by randomly creating a starting population. The number of individuals can impact the diversity of the explored design space and the convergence time of the algorithm. Larger populations provide a greater genetic diversity, but could yield to a slower execution time.
- *Sorting*: The particular feature of the elitist algorithm, compared to a common genetic algorithm, is to improve the diversity of the individuals. Before proceeding with the reproduction and mutation processes for the creation of the next generation of the population, each individual of the current population is marked by a fitness value, namely a *rank*. As shown in Fig. 5.3, for each algorithm iteration, at the set of non-dominated solutions is assigned the highest fitness value, or *rank 0*. The *rank* i^{th} definition can be iteratively applied, by defining the individuals of the generic i^{th} rank as the ones only dominated by the individuals belonging to the $(i-1)^{th}$ rank. It is clear that the genomes with better rank have a larger probability to have better genes, hence they are more likely to be selected for the next generation. Nevertheless, the NSGA II keeps a certain diversity among the solutions and prevents an excessive crowding of solutions with same rank through a Crowding function. A distance measure function, indeed, is performed in order to classify the solutions depending on their distance from the others genomes [147]. Within the same rank, the solutions are more likely to be selected in the next generation. It shall be underlined that the constraints functions, contrarily to the genetic algorithm, intervene in the ranking process of the solutions, so that the unfeasible solutions are assigned to the higher rank [147] and discarded in the parent selection step.
- *Reproduction and Mutation*: Once the parent (current) generation individuals are classified by their fitness value and the distance function within each rank, the algorithm randomly selects the parents of the future generation children. The size of the generated population is equal to the parent one. However, the user can define the ratio between the number of individuals generated by crossover (or reproduction) and the ones generated by mutation. The "Creation Function" for the generation of the first population, the "Mutation Function" and the "Crossover Function" can be set among the available functions or customized at will.

Among the several crossover procedure possible, the intermediate function have been employed for the considered problem. Once the two parents $\boldsymbol{x}_{parent_1}$ and $\boldsymbol{x}_{parent_2}$ are selected among the parent generation, each child $\boldsymbol{x}_{child}$ is evaluated by a random weighted average of the parents:

$$\boldsymbol{x}_{child} = \boldsymbol{x}_{parent_1} + \alpha_{cr}(\boldsymbol{x}_{parent_1} + \boldsymbol{x}_{parent_2})$$

where α_{cr} is a random number in the range $[0, 1]$.

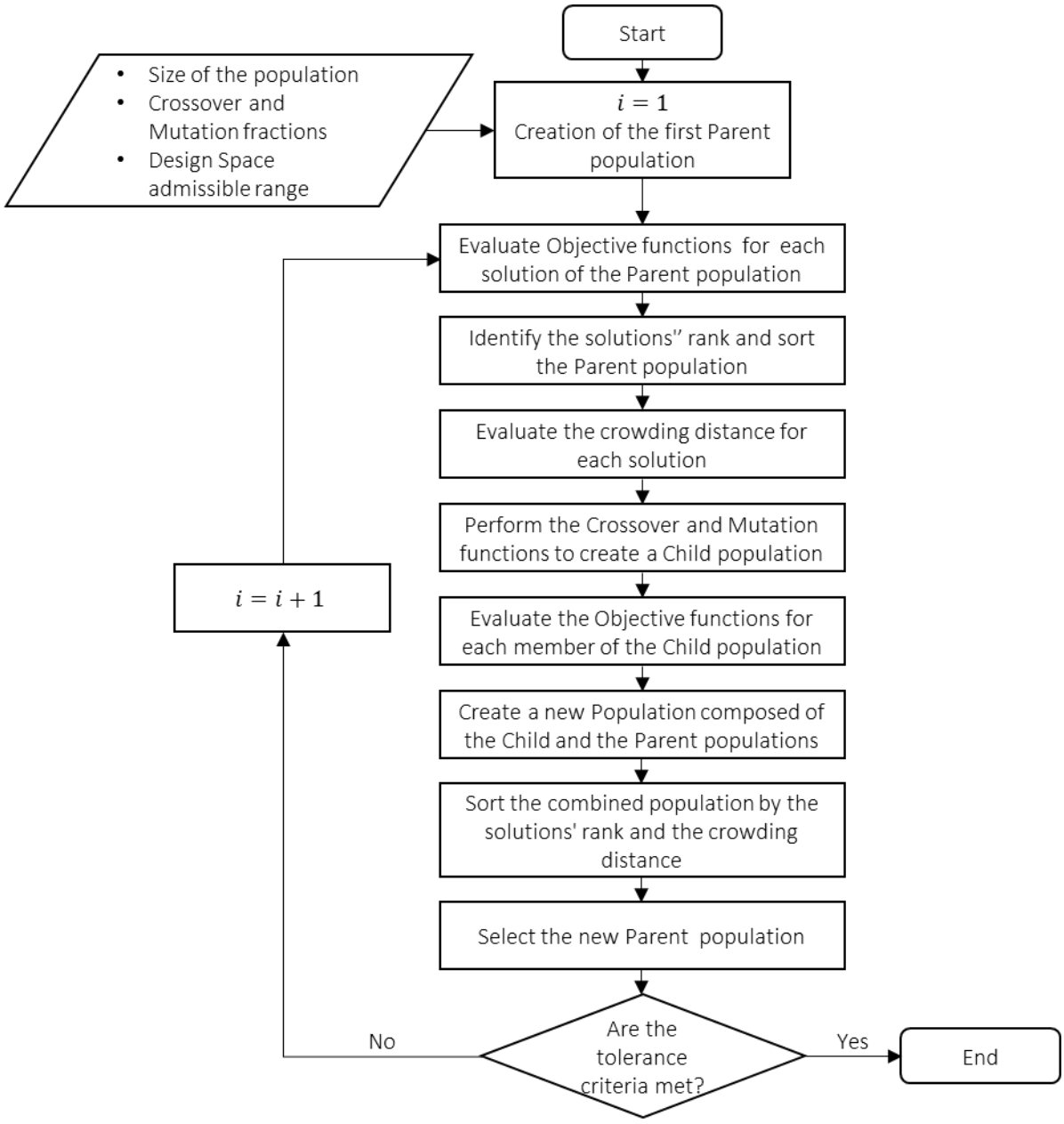


Fig. 5.2 NSGA II flowchart.

The mutation process performs random changes in the individuals genes in the population, so improving the genetic diversity. As for the crossover process, several functions are available in literature, but only the Gaussian one will be described. A random number α_m multiplied by the range interval $[\boldsymbol{x}_{UB}(i) - \boldsymbol{x}_{LB}(i)]$ of the i^{th} variable is added to each variable of the mutating solution:

$$\boldsymbol{x}_{child}(i) = \boldsymbol{x}_{parent}(i) + \alpha_m(\boldsymbol{x}_{UB}(i) - \boldsymbol{x}_{LB}(i))$$

where $\boldsymbol{x}_{LB}$ and $\boldsymbol{x}_{UB}$ represent respectively the lower and upper vector boundaries that limit the range in which the $\boldsymbol{x}$ solutions may vary. The value of the coefficient $\alpha_m \in [0, 1]$ is randomly generated accordingly to a Gaussian distribution centred in zero, with a tuneable standard deviation (scale factor). The algorithm may imply even a progressive shrinking of such standard deviation at each generation.

- *Selection*: After obtaining as many children as parents, the algorithm evaluates the respective objective functions values and sorts the new population composed of parents and children, as explained in the step "*Sorting*".
  Once the two generations are ready and classed according to the criteria mentioned above, the algorithm chooses the best elements among the two generations of parents and children, by replacing the worst design solutions in the child population with the best design in the parent population. A new generation is created and the iteration ends.

The iteration may stop after reaching a pre-set number of iterations or a certain amount of time. In the NSGA II, another stopping criterion is provided by the Spread function: since the main interest is to find a solution set which lies within the Pareto optimal region, the Spread function measures the extent of the spread achieved among the obtained solutions by averaging the consecutive Euclidean distances of the Pareto front obtained. When the difference between the spread values evaluated for two sets of Pareto solutions obtained in two consecutive iterations goes below an assigned value, called "Function Tolerance", the algorithm stops.

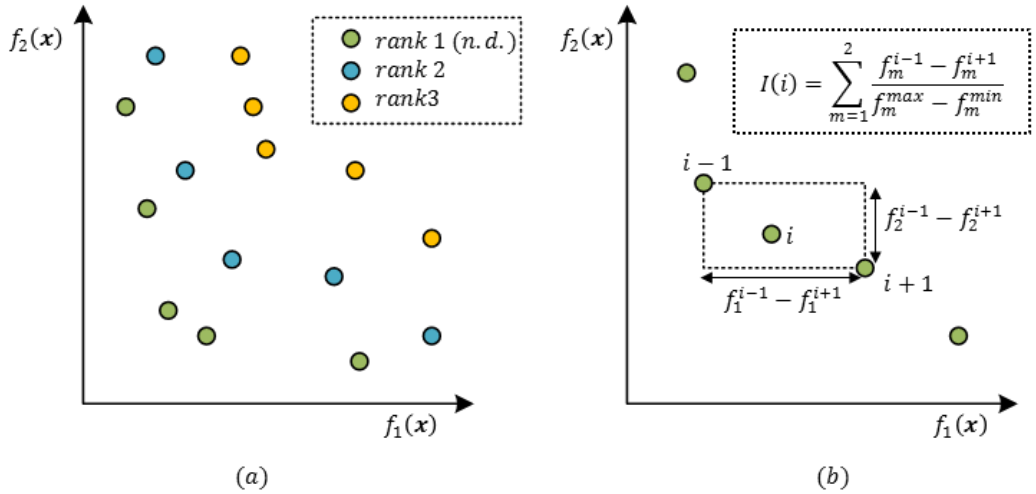


Fig. 5.3 Ranking of the population (a) and evaluation of the crowding distance $I(i)$ relative to the i^{th} element within the same rank of solutions (b).

5.2 Multi-objective optimization of a DC/DC converter

The algorithm has been performed to optimize a DC/DC step-up converter for a motor drive application. The main goals of the optimization were to improve the efficiency and the compactness of the converter. The objective functions to minimize will be then represented by the total power losses and the total volume of the converter. In this chapter, two different optimization will be performed.

The optimization is performed on a standard boost converter. The objective is to optimize the converter for an application that complies with the specifications not only in steady state, but also during load transient events. In order to optimize size and efficiency of the converter and guarantee a good rejection of the load transients, the design of both the power stage and the controller parameters should be treated

simultaneously. If the mission profile includes variations of the operating point, the converter should be designed to fulfil these transients without exceeding the design specifications.

Table 5.1 Design specifications.

Symbol	Description	Value
V_{in}	Input voltage	270 V
V_o	Output voltage	350 V
P_o	Load power	[0–3kW]
$\Delta v_o^{(steady)} = \Delta v_o^{(LT)}$	Output voltage ripple limit	2% V_o
$\Delta i_{in_{lim}}$	Input current ripple limit	14% I_{in}

The operating point and the application requirements are described in Table 5.1. The converter is designed for a nominal power of $P_o = 3kW$. The specification concerning the output voltage excursion has been assumed equal to the steady-state ripple $\Delta v_o^{(steady)} = \Delta v_o^{(LT)}$. As stated in the DO-160F standards [23], it has been assumed a steady state input ripple constraint for the D category power converters (270V input voltage with a load power [1kW, 10kW]). Moreover, in order to prevent instability issues due to the interaction between the input filter and the controlled system, the routine includes a constraint function to prevent the instability of the Pareto design solutions. The algorithm assigns the maximal rank to the unfitting solutions and discards them.

All the optimization routines have been performed on a workstation with CPU E5-1660 v4 Intel® Xeon® @3.20 GHz, RAM 64Gb. For the optimization problem considered, the routine was performed through an implemented function *gamultiobj.m* in MATLAB environment [152], based on the NSGA II. The parameters relative to the performed routines are reported in Table 5.2.

Table 5.2 NSGA-II algorithm parameters.

Description	Value
Initial population	400
Crossover Fraction	0.6
Mutation Factor	0.4
Crossover Function	'Intermediate'
Mutation Function	'Uniform'
Tolerance factor on spread average variation	$1e^{-4}$
Pareto Fraction	0.35
Optimization time	< 27h
Iterations number	< 150

When performed on the mentioned workstation, the evaluation time of the routine did not exceed the 27 hours and the 150 in the worst case. The processing time is mostly due to the stability constraint function, since it requires about $5s$ to perform each stability check. If the stability constraint function is excluded from the routine, the evaluation time is reduced to 4 hours (in the worst case).

In all cases, the algorithm stops because the stopping criterion concerning the Pareto spread tolerance value is satisfied.

As already mentioned, prior to discussing the optimizations' routines results, the design space and the objective functions shall be clearly defined.

5.2.1 Design Space and parameters

Depending on the degrees of freedom of the problem, a set of independent variables should be arbitrarily chosen in order to define the genome of the design solution. In (5.7), the design variables have been assumed to be continuous values belonging to the real number's domain.

For the considered problem, only values related to available components (semiconductor switches, inductor cores and capacitors…) on the market should be considered, so that parameters and variables are no longer continuous but can assume only discrete values.

The available components have been organized and indexed along with the respective parameters in spreadsheets. Rather than directly dealing with the parameters values stemming from the components' datasheets, it has been preferred to employ discrete variables which correspond to the reference indexes of the available components in the spreadsheet, in order to easily attain all the relative parameters. The creation, crossover and mutation functions have been accordingly modified in order to specifically deal with discrete values.

The independent variables selected for the composition of the individual genome are described below:

- The *switching frequency* f_s is one of the most influent parameters in the design of a SMPS. It affects directly the current ripple Δi_L through the inductors and the voltage ripple across the capacitors, hence their inductance and capacitance values and their volume, as explained in Chapter 3. It has a remarkable impact on the core losses and the switching losses of the active switches. Furthermore, the switching frequency appears as a limiting factor of the controller bandwidth, as it will be explained.
- *Inductors parameters*: The design of the magnetic components has been discussed in Chapter 3. The inductance value depends on the number of turns n_L, the geometric dimensions of the core and the relative permeability of the core. The equation (3.39) in Section 3.4.1, which defines the inductance value, has three degrees of freedom (the geometric dimensions of the core A_{core} and l_m are related to the same core and its index, hence they cannot be accounted as two separate degrees of freedom). As already mentioned, the core material of the inductors is a ferrous alloy powder with distributed air gap from Magnetics, which are featured by low core power losses [105]. These are un-gapped toroidal cores with several available values of magnetic permeability. The boost inductor *L* may require a large inductance value, then High Flux series cores were considered as the most appropriate because of their high available biasing capability. Then a smaller magnetic core can be used because of the high flux density saturation limit. As for the L_{fil} input filter inductor, Molypermalloy (MPP) cores were chosen for the superior performances at high frequencies. The spreadsheets relative to the magnetic cores and their parameters are shown in Fig. 5.5 and Fig. 5.6. For each inductor (namely the boost inductor and input filter inductor), indeed, the number of turns n_L and $n_{L_{fil}}$, the index of the magnetic cores In_L and $In_{L_{fil}}$ and the indexes In_{μ_L} and $In_{\mu_{L_{fil}}}$ of the available values of relative permeability are assumed as independent design variables.
  Each index In_L and $In_{L_{fil}}$ is associated to the geometrical dimensions (A_{core}, l_m, and thickness and size of the outer and internal diameters for the evaluation of the coils length MLT) of an available magnetic core in for the High Flux cores, in Fig. 5.5 for the MPP cores.

In_L	Ref.	l_m Path Length	A_c Cross Section	Volume	Outer diameter	Internal diameter	Thickness
		mm	mm2	mm3	mm	mm	mm
1	150	9.42	2.11	19.88	4.57	1.73	3.18
2	180	10.62	2.85	30.27	5.29	1.85	3.18
3	20	13.61	4.82	65.6	6.99	2.29	3.43
4	240	13.63	4.76	64.9	7.06	2.16	3
5	270	13.63	9.12	124.3	7.24	2.16	5.41
6	410	16.5	7.25	119.6	7.32	3.63	5.72
7	30	17.9	6.02	107.8	8.51	3.45	3.81
8	280	21.8	7.51	163.7	10.3	4.27	3.81
9	290	21.8	9.45	206	10.3	4.27	4.6
10	40	23	9.76	225	10.8	4.57	4.6
11	130	26.9	9.27	249	11.8	5.84	4.6
12	50	31.2	11.7	365	13.5	6.99	5.51
13	120	41.2	19.56	806	17.3	9.53	7.11
14	380	41.4	23.2	960	18	9.02	7.11
15	206	50.9	23.47	1194	21.1	12.1	7.11
16	310	56.7	32.85	1863	23.6	13.3	8.4
17	350	58.8	38.8	2281	24.3	13.8	9.7
18	930	65.4	66.1	4322	27.7	14.1	11.9
19	548	81.4	67.7	5509	33.8	19.3	11.4
20	585	89.5	47.1	4215	35.2	22.6	9.8
21	324	89.8	68.3	6136	36.7	21.5	11.4
22	254	98.4	110.6	10880	40.8	23.3	15.4
23	89	116.3	133.3	15502	47.6	27.9	16.1
24	438	107.4	197.7	21235	47.6	23.3	18.9
25	725	114	262	29700	51.31	23.9	21.6
26	715	127.3	124.4	15832	51.7	30.9	14.4
27	109	143	146.3	20918	58	34.7	14.9
28	195	125	229	28625	58	25.6	16.1
29	620	144	360	51800	62.9	31.7	25.9
30	70	158	314	49700	69.4	34.7	21.4
31	778	170	478	81500	78.9	38.3	26.8
32	740	184	497	91400	75	44.4	35.9
33	866	196	176	34500	78.9	48.2	13.9
34	906	196	221	43400	78.9	48.2	17.1
35	102	243	358	86900	103	55.8	17.9
36	337	324	678	220000	134	77.2	26.8
37	165	412	987	407000	166.5	101	33.15

Fig. 5.4 Magnetics High Flux cores reference codes and geometric dimensions data [104].

$In_{L_{fil}}$	Ref.	l_m path Length	A_cCross Section	Volume	Outer diameter	Internal diameter	Thickness
		mm	mm^2	mm^3	mm	mm	mm
1	140	8.06	1.3	10.48	4.19	1.27	2.16
2	150	9.42	2.11	19.88	4.57	1.73	3.18
3	180	10.62	2.85	30.27	5.11	2.03	3.18
4	20	13.61	4.82	65.6	6.99	2.29	3.43
5	240	13.63	4.76	64.9	7.06	2.16	3
6	270	13.63	9.12	124.3	7.24	2.16	5.41
7	410	16.5	7.25	119.6	7.32	3.63	5.72
8	30	17.9	6.02	107.8	8.51	3.45	3.81
9	280	21.8	7.51	163.7	10.3	4.27	3.81
10	290	21.8	9.45	206	10.3	4.27	4.6
11	40	23	9.76	225	10.8	4.57	4.6
12	130	26.9	9.27	249	11.8	5.84	4.6
13	50	31.2	11.7	365	13.5	6.99	5.51
14	120	41.2	19.56	806	17.3	9.53	7.11
15	380	41.4	23.2	960	18	9.02	7.11
16	206	50.9	23.47	1194	21.1	12.1	7.11
17	310	56.7	32.85	1863	23.6	13.3	8.4
18	350	58.8	38.8	2281	24.3	13.8	9.7
19	930	65.4	66.1	4322	27.7	14.1	11.9
20	548	81.4	67.7	5509	33.8	19.3	11.4
21	585	89.5	47.1	4215	35.2	22.6	9.8
22	324	89.8	68.3	6136	36.7	21.5	11.4
23	254	98.4	110.6	10880	40.8	23.3	15.4
24	89	116.3	133.3	15502	47.6	27.9	16.1
25	438	107.4	197.7	21235	47.6	23.3	18.9
26	725	114	262	29700	51.3	23.9	21.6
27	715	127.3	124.4	15832	51.7	30.9	14.4
28	109	143	146.3	20918	58	34.7	14.9
29	195	125	229	28625	58	25.6	16.1
30	620	144	360	52000	62.9	31.7	25.9
31	70	158	314	49700	69.4	34.7	21.4
32	778	170	478	81500	78.9	38.3	26.8
33	740	184	497	91400	74.1	45.3	35
34	866	199.5	176	35112	78.9	48.2	13.8
35	906	199.5	227	45287	78.9	48.2	17
36	102	243	358	86900	103	55.8	17.9
37	337	324	678	220000	134	77.2	26.8

Fig. 5.5 Magnetics MPP cores reference codes and geometric dimensions data [103].

The In_{μ_L} and $In_{\mu_{L_{fil}}}$, besides referring to the relative magnetic permeability values, are employed to address the Steinmetz parameter k_{fe} ,α and β relative to each material in Fig. 5.6, required for the evaluation of the magnetic cores losses (Section 3.4.1.3).

- *Switching devices parameters*: the switching device has a remarkable impact on the converter power losses and on the choice of the switching frequency. The MOSFETs and their respective parameters are selected among available SiC based components produced by ROHM and Wolfspeed (CREE) manufacturers with suitable ratings ($i_{DS_{max}}(@150°C) \in [20A, 100A]$, $v_{DS_{max}}$>500V). The MOSFETs are chosen between 29 components, whose references and relative parameters are listed in Fig. 5.7. From the datasheet of each MOSFET, all the parameters required for the evaluation of the power losses and the cooling system design are extracted and employed in the algorithm (current rating, threshold gate-source voltage, parallel diode conduction voltage, trans-conductance gain, internal gate resistance, intrinsic capacitances, gate-source and gate-drain capacitors switching charges, reverse recovery charge of the parallel diode and thermal resistance from the junction to the case). All those parameters are determined at the junction temperature of $T_j = 125°C$.
  The index In_{MOS}, employed as design variable, relates to a specific SiC MOSFET and its respective parameters.

In_{μ_L}	μ	k_{fe}	α	β
1	14 μ_0	115.9	2.5	1.87
2	26 μ_0	70.83	2.34	1.65
3	60 μ_0	357.1	2.05	1.12
4	125 μ_0	53.05	2.06	1.56
5	147 μ_0	52.16	2	1.57
6	160 μ_0	52.16	2	1.57
7	173 μ_0	52.16	2	1.57
8	200 μ_0	37.97	2.09	1.68
9	300 μ_0	37.97	2.09	1.68

(a)

$In_{\mu_{L_{fil}}}$	μ	k_{fe}	α	β
1	14 μ_0	388.8	2.31	1.54
2	26 μ_0	374.9	2.21	1.49
3	40 μ_0	492	2.22	1.32
4	60 μ_0	492	2.22	1.32
5	125 μ_0	246	2.23	1.47
6	147 μ_0	447.6	2.3	1.41
7	160 μ_0	447.6	2.3	1.41

(b)

Fig. 5.6 Steinmetz parameters for MPP(a) and High flux (b) Magnetic powder cores materials [103], [104].

The parameters set $[n_L, In_L, In_{\mu_L}, n_{L_{fil}}, In_{L_{fil}}, In_{\mu_{L_{fil}}}, f_s, In_{MOS}]$, stands for the independent variables genome. It should be noted that the assortment of the active and passive components can be changed or extended depending on the experience and preferences of the designer, without bringing any modification to the optimization procedure.

It is worth remarking that the output and the filter capacitors do not appear among the independent variables, since they can be evaluated from the data provided by the genome alone.

The C_{fil} value can be obtained by (3.75) and (3.76) in Chapter 3, once the Δi_L current ripple and the attenuation required by the filter have been evaluated for the steady state condition.

As explained in Section 3.4.2, the C_o minimal value for the compliance to the steady state voltage ripple specification, can be deducted by the operating point data, ripple constraint, switching frequency and L inductance value for the steady state case. Concerning the compliance with the voltage excursion specification $\Delta v_o^{(LT)}$ in load transient conditions, the design of the capacitor value C_o for each design solution requires the knowledge of the control law and its parameters, as discussed in Section 4.5. The control strategy consists of the double loop architecture composed by a peak current inner controller and an outer controller which regulates the electrostatic energy in C_o. The k_i and k_p parameters of the control law are defined as:

$$k_p = 2\,\zeta\omega_e, k_i = \omega_e^2\,, \omega_e = \omega_{f_s}/F_{\omega_e} \tag{5.15}$$

where ζ and ω_e are respectively the damping factor and the cut-off angular frequency of the controlled system. In order to avoid any interaction between the inner and the outer controllers, ω_e is chosen lower than the switching angular frequency ω_{f_s} of a factor F_{ω_e}, according to (5.15).

The capacitors' design for each independent parameters set leads to the determination of the index values relative to the closest available capacitors, chosen among the film Vishay MKP1848C DC-Link series [153], with a voltage rating of 500V, listed in Fig. 5.8 along with the respective volumes and series resistances.

In_{MOS}	Manufacturer	Reference	I_{max} (100°)	V_{th}	V_d f.w. Diode voltage	r_{DS}	κ_{ch}	$R_{gate}^{(int)}$	C_{oss}	Qsw ($Q_{GD}+Q_{GS}$)	Q_{rr}	$R_{th_{j-c}}$	$R_{th_{c\_h}}$	$Qsw \times r_{DS}$
1	CREE	C2M0280120D	$2.00E+01$	$2.10E+00$	$3.60E+00$	$5.30E-01$	$6.12E-01$	$1.14E+01$	$2.30E-11$	$1.04E-08$	$7.00E-08$	$2.00E+00$	$2.00E-01$	$5.51E-09$
2	ROHM	SCT3080AL	$2.10E+01$	$2.70E+00$	$3.20E+00$	$1.06E-01$	$2.49E-01$	$1.30E+01$	$3.90E-11$	$2.40E-08$	$5.30E-08$	$1.12E+00$	$2.00E-01$	$2.53E-09$
3	ROHM	SCT3080ALHR	$2.10E+01$	$2.70E+00$	$3.20E+00$	$1.15E-01$	$2.52E-01$	$1.30E+01$	$3.90E-11$	$3.00E-08$	$5.30E-08$	$1.12E+00$	$2.00E-01$	$3.45E-09$
4	CREE	C3M0065090J	$2.20E+01$	$1.60E+00$	$4.40E+00$	$9.00E-02$	$3.03E+00$	$4.70E+00$	$6.00E-11$	$1.58E-08$	$2.45E-07$	$1.10E+00$	$2.00E-01$	$1.42E-09$
5	ROHM	SCT3080KLHR	$2.20E+01$	$2.70E+00$	$3.20E+00$	$1.36E-01$	$2.52E-01$	$1.20E+01$	$7.50E-11$	$3.65E-08$	$5.00E-08$	$9.10E-01$	$2.00E-01$	$4.96E-09$
6	CREE	C3M0065100K	$2.25E+01$	$1.60E+00$	$4.40E+00$	$9.00E-02$	$3.03E+00$	$4.70E+00$	$6.00E-11$	$2.05E-08$	$3.10E-07$	$1.10E+00$	$2.00E-01$	$1.85E-09$
7	CREE	C3M0065100J	$2.25E+01$	$1.60E+00$	$4.40E+00$	$9.00E-02$	$3.03E+00$	$4.70E+00$	$6.00E-11$	$2.05E-08$	$3.10E-07$	$1.10E+00$	$2.00E-01$	$1.85E-09$
8	CREE	E3M0065090D	$2.30E+01$	$1.60E+00$	$4.40E+00$	$9.00E-02$	$3.03E+00$	$4.70E+00$	$6.00E-11$	$1.58E-08$	$1.50E-07$	$1.00E+00$	$2.00E-01$	$1.42E-09$
9	CREE	E3M0120090D	$2.30E+01$	$1.60E+00$	$4.40E+00$	$1.70E-01$	$1.52E+00$	$1.60E+01$	$4.00E-11$	$7.40E-09$	$1.15E-07$	$1.30E+00$	$2.00E-01$	$1.26E-09$
10	CREE	C3M0065090D	$2.30E+01$	$1.60E+00$	$4.40E+00$	$9.00E-02$	$3.03E+00$	$4.70E+00$	$6.00E-11$	$1.58E-08$	$1.50E-07$	$1.00E+00$	$2.00E-01$	$1.42E-09$
11	CREE	C2M0080120D	$2.40E+01$	$2.10E+00$	$3.10E+00$	$1.28E-01$	$1.69E+00$	$4.60E+00$	$8.00E-11$	$3.05E-08$	$1.92E-07$	$6.50E-01$	$2.00E-01$	$3.90E-09$
12	CREE	C2M0080170P	$2.70E+01$	$2.00E+00$	$3.60E+00$	$1.50E-01$	$5.00E+00$	$2.00E+00$	$1.05E-10$	$4.70E-08$	$1.00E-06$	$4.50E-01$	$2.00E-01$	$7.05E-09$
13	ROHM	SCT3060ALHR	$2.70E+01$	$2.70E+00$	$3.20E+00$	$8.60E-02$	$2.52E-01$	$1.20E+01$	$5.50E-11$	$3.65E-08$	$5.50E-08$	$9.10E-01$	$2.00E-01$	$3.14E-09$
14	ROHM	SCH2080KE	$2.80E+01$	$1.60E+00$	$1.30E+00$	$1.25E-01$	$3.65E-01$	$6.30E+00$	$1.75E-10$	$4.45E-08$	$6.00E-08$	$5.70E-01$	$2.00E-01$	$5.56E-09$
15	ROHM	SCT2080KEHR	$2.80E+01$	$1.60E+00$	$4.60E+00$	$1.25E-01$	$3.43E-01$	$6.30E+00$	$7.70E-11$	$4.45E-08$	$4.40E-08$	$5.70E-01$	$2.00E-01$	$5.56E-09$

16	ROHM	SCH2080KE	$2.90E+01$	$1.60E+00$	$4.30E+00$	$1.49E-01$	$2.19E-01$	$1.38E+01$	$1.75E-10$	$2.80E-08$	$5.30E-08$	$9.10E-01$	$2.00E-01$	$4.17E-09$
17	ROHM	SCT3040KLHR	$3.90E+01$	$2.70E+00$	$3.20E+00$	$6.80E-02$	$5.34E-01$	$7.00E+00$	$7.60E-11$	$6.45E-08$	$1.15E-07$	$5.70E-01$	$2.00E-01$	$4.39E-09$
18	CREE	C3M0030090K	$4.00E+01$	$1.70E+00$	$4.50E+00$	$3.70E-02$	$6.06E+00$	$3.00E+00$	$1.31E-10$	$3.95E-08$	$5.45E-07$	$8.40E-01$	$2.00E-01$	$1.46E-09$
19	CREE	C2M0040120D	$4.00E+01$	$2.10E+00$	$3.10E+00$	$8.40E-02$	$2.27E+00$	$1.80E+00$	$1.50E-10$	$5.10E-08$	$2.83E-07$	$3.80E-01$	$2.00E-01$	$4.28E-09$
20	CREE	C2M0045170P	$4.80E+01$	$1.80E+00$	$3.60E+00$	$9.00E-02$	$7.81E+00$	$1.30E+00$	$1.71E-10$	$7.90E-08$	$2.00E-06$	$2.40E-01$	$2.00E-01$	$7.11E-09$
21	CREE	C2M0045170D	$4.80E+01$	$1.80E+00$	$3.60E+00$	$9.00E-02$	$7.81E+00$	$1.30E+00$	$1.71E-10$	$7.90E-08$	$5.30E-07$	$2.40E-01$	$2.00E-01$	$7.11E-09$
22	ROHM	SCT3030ALHR	$4.90E+01$	$2.70E+00$	$3.20E+00$	$4.30E-02$	$5.34E-01$	$7.00E+00$	$8.90E-11$	$6.45E-08$	$1.30E-07$	$5.70E-01$	$2.00E-01$	$2.77E-09$
23	CREE	C2M0025120D	$6.00E+01$	$2.10E+00$	$3.10E+00$	$4.30E-02$	$8.16E+00$	$1.10E+00$	$2.20E-10$	$7.30E-08$	$4.06E-07$	$2.70E-01$	$2.00E-01$	$3.14E-09$
24	ROHM	SCT3022AL	$6.50E+01$	$2.70E+00$	$3.20E+00$	$2.90E-02$	$7.12E-01$	$5.00E+00$	$1.18E-10$	$6.85E-08$	$1.46E-07$	$4.40E-01$	$2.00E-01$	$1.99E-09$
25	ROHM	SCT3022KL	$6.70E+01$	$2.70E+00$	$3.20E+00$	$3.30E-02$	$7.12E-01$	$4.00E+00$	$2.37E-10$	$1.00E-07$	$1.75E-07$	$3.50E-01$	$2.00E-01$	$3.30E-09$
26	ROHM	SCT2080KLHR	$6.70E+01$	$2.70E+00$	$3.20E+00$	$3.80E-02$	$7.12E-01$	$4.00E+00$	$7.70E-11$	$1.10E-07$	$1.75E-07$	$3.50E-01$	$2.00E-01$	$4.18E-09$
27	CREE	C3M0075120K	$8.00E+01$	$2.00E+00$	$4.00E+00$	$1.00E-01$	$4.00E+00$	$1.05E+01$	$5.80E-11$	$2.80E-08$	$2.20E-07$	$1.10E+00$	$2.00E-01$	$2.80E-09$
28	CREE	C3M0075120J	$8.00E+01$	$2.00E+00$	$3.75E+00$	$1.00E-01$	$5.00E+00$	$1.05E+01$	$5.80E-11$	$2.80E-08$	$2.20E-07$	$1.10E+00$	$2.00E-01$	$2.80E-09$
29	ROHM	BSM08012P2C008	$8.00E+01$	$1.60E+00$	$2.30E+00$	$6.80E-02$	$9.77E-01$	$3.00E+00$	$6.00E-10$	$1.40E-07$	$2.70E-10$	$3.20E-01$	$3.50E-02$	$9.52E-09$

Fig. 5.7 MOSFETs spreadsheet with the respective parameters.

Reference	V	$C(\mu F)$	$w(mm)$	$h(mm)$	$l(mm)$	$V(m\text{^}3)$	$ESR(\Omega)$
MKP1848C51050JK2	500	1	9	19	32	$5.472E-06$	0.09
MKP1848C52050JK2	500	2	9	19	32	$5.472E-06$	0.045
MKP1848C53050JK2	500	3	9	19	32	$5.472E-06$	0.03
MKP1848C54050JK2	500	4	11	21	32	$7.392E-06$	0.023
MKP1848C55050JK2	500	5	11	21	32	$7.392E-06$	0.018
MKP1848C56050JK2	500	6	13	23	32	$9.568E-06$	0.015
MKP1848C57050JK2	500	7	15	25	32	0.000012	0.013
MKP1848C58050JK2	500	8	15	25	32	0.000012	0.012
MKP1848C59050JK2	500	9	18	28	32	$1.6128E-05$	0.011
MKP1848C61050JK2	500	10	18	28	32	$1.6128E-05$	0.01
MKP1848C61250JK2	500	12	18	28	32	$1.6128E-05$	0.008
MKP1848C61550JK2	500	15	21	31	32	$2.0832E-05$	0.007
MKP1848C61850JK2	500	18	20	35	32	0.0000224	0.006
MKP1848C62050JP*	500	20	18.5	35.5	43	$2.824E-05$	0.009
MKP1848C62250JP*	500	22	21.5	38.5	43	$3.5593E-05$	0.009
MKP1848C62550JP*	500	25	21.5	38.5	43	$3.5593E-05$	0.008
MKP1848C63050JP*	500	30	24	44	42	$4.4352E-05$	0.007
MKP1848C63550JP*	500	35	24	44	42	$4.4352E-05$	0.006
MKP1848C64050JP*	500	40	30	45	42	0.0000567	0.005
MKP1848C64550JP*	500	45	30	45	42	0.0000567	0.0045
MKP1848C65050JP*	500	50	30	45	42	0.0000567	0.004
MKP1848C65550JP*	500	55	30	57	42	0.00007182	0.0035
MKP1848C66050JP*	500	60	30	57	42	0.00007182	0.0035
MKP1848C66550JP*	500	65	30	57	42	0.00007182	0.0025
MKP1848C65050JY*	500	50	25	45	57.5	$6.4688E-05$	0.007
MKP1848C65550JY*	500	55	25	45	57.5	$6.4688E-05$	0.007
MKP1848C66050JY*	500	60	30	45	57.5	$7.7625E-05$	0.006
MKP1848C66550JY*	500	65	30	45	57.5	$7.7625E-05$	0.006
MKP1848C67050JY*	500	70	30	45	57.5	$7.7625E-05$	0.006
MKP1848C67550JY*	500	75	35	50	57.5	0.00010063	0.005
MKP1848C68050JY*	500	80	35	50	57.5	0.00010063	0.0045
MKP1848C69050JY*	500	90	35	50	57.5	0.00010063	0.004
MKP1848C71050JY*	500	100	35	50	57.5	0.00010063	0.004
MKP1848C71150JY5	500	110	45	45	57.5	0.00011644	0.0025
MKP1848C71250JY5	500	120	45	45	57.5	0.00011644	0.0025
MKP1848C72550JY5	500	250	70	65	57.5	0.00026163	0.002
MKP1848C75050JY5	500	500	130	65	57.5	0.00048588	0.0015

Fig. 5.8 MKP1848 capacitors spreadsheet, with geometrical dimensions and series resistance [153].

The design optimization involves several parameters that are assumed constant during the iterations, depicted in Table 5.3 for the considered case.

Table 5.3 Optimization parameters.

Description	Value
Gate resistance (for the switching losses evaluation)	$R_{gate} = [4\Omega, 16\Omega]$
Dead time (for the free-wheeling diode losses evaluation)	$t_{dead} = 0.5\mu s$
Wire section (for the evaluation of the copper losses in the inductors windings)	$A_{wire} = 0.79mm^2$
Control law damping factor (5.15)	$\zeta = 0.7$
Switching frequency-controller bandwidth ratio (5.15)	$F_{\omega_e} = 50$
Environment temperature (for the heatsink design)	$T_a = 25°C$

The gate resistance R_{gate} could play a relevant role in the design of a SMPS converter. As showed in Chapter 3, it has an important impact on the switching times of the semiconductor devices, hence on their power losses. Smaller the switching times, higher the efficiency performance. That means that it is possible to reduce the heatsink volume or/and increase the switching frequency, which allows to reduce the passive components. Nevertheless, it has been considered as an optimization parameter, rather than a design variable, because the algorithm would have clearly provided Pareto solutions with $R_{gate} = 0$, since it ensures the lowest power losses, and so the highest switching frequency. On the other hand, as explained in Chapter 1, low values of R_{gate} provoke steeper slopes of both current and voltage across the switching device, resulting in greater harmonic content. The harmonic content provokes dangerous ringing phenomena that could compromise the reliability of the same converter. Moreover, it leads to the choice of a bulkier EMI filter for the rejection of the high frequency content conducted toward the DC bus. To take into account such trade-off (efficiency, size, reliability and EMI issues), it is required a figure of merit that could take into account the EMI impact on the converter and its design (through a high frequency model of the converter, for example), which is pretty challenging to obtain. Then, the algorithm has been executed for several values of the gate resistance R_{gate}, which impose different transistors' switching times.

5.2.2 Objective functions

The considered objective functions, namely volume and power losses, are detailed in this section.

The volume function includes the volume of the passive components $(C_{fil}, C_o, L_{fil}, L)$ and of the heatsink:

$$V_{(converter)} = V_{(L)} + V_{(L_{fil})} + V_{(C_o)} + V_{(C_{fil})} + V_{(heatsink)} \tag{5.16}$$

The volume of each passive element is derived from the capacitors and the corresponding index defined in the previous section.

The heatsink volume is deduced through the data provided by the manufacturer and from the required thermal resistance $R_{th_{h-a}}$, for a maximal junction temperature of $T_j = 125°C$. At each MOSFET index In_{MOS} corresponds a value of the junction-case thermal resistance $R_{th_{j-c}}$, and a value of the case-

heatsink interface thermal resistance $R_{th_{c-h}}$, both extracted from the MOSFETs spreadsheet in Fig. 5.7. The required thermal resistance $R_{th_{h-a}}$ can be then evaluated by (3.36) in Chapter 3.

By fitting the provided thermal resistance values in case of natural convection, an exponential relation between the volume of the heatsink $V_{(heatsink)}$ and the thermal resistance $R_{th_{h-a}}$ was modelled for the ABL 118AB heatsink series [154], as explained in Section 3.3.4.

The power losses objective function includes the MOSFETs' (S_1 and S_2) and the inductors' power losses (L and L_{fil}) and the capacitor losses (C_o and C_{fil}):

$$P_{(converter)} = P_{(L)} + P_{(L_{fil})} + P_{MOS(S_1)} + P_{MOS(S_2)} + P_{diode(S_2)} + P_{(C_o)} + P_{(C_{fil})} \tag{5.17}$$

The switches power losses model discussed in Chapter 3, includes both switching and conduction losses as well as the diode's losses:

$$P_{MOS(S_i)} = P_{on}^{(S_i)} + P_{off}^{(S_i)} + P_{(conduction)}^{(S_i)} \tag{5.18}$$

The inductors' losses $P_{(L)}$ and $P_{(L_{fil})}$ include the power losses in the copper coils $P_{(copper)}^{(L)}$ and in the magnetic core $P_{(core)}^{(L)}$:

$$P_{(L)} = P_{(copper)}^{(L)} + P_{(core)}^{(L)} \tag{5.19}$$

They are computed according to (3.57) and (3.65), as explained in Chapter 3.

The terms $P_{(C_o)}$ and $P_{(C_{fil})}$ represent the power losses due to the ESR series resistances of the capacitors C_o and C_{fil}, available in the spreadsheet in Fig. 5.8.

As explained in Section 5.1.1, according to the applications requirements, the objective functions can be modified or differently chosen without compromising the validity of this study.

5.2.3 Constraints Functions

At each iteration the optimization solver includes a non-linear constraint function, whose purpose is to discard the unfeasible solutions. Indeed, the design solution should respect technological and behavioural constraints.

The constraint functions concerns three aspects. First, it includes the inductors design constraints, namely the saturation of the inductors magnetic cores and the limit number of coils n_L due to the finite winding area W_A. Second, it addresses the maximal current through the switches. Third, concerning the second optimization, it deals with the stability criterion.

As for the inductor aspect, the following conditions must be met:

$$B_{L_{max}}\left(i_{L_{max}}\right) \leq 0.8\, B_{sat}^{(HFlux)} \tag{5.20}$$

$$B_{L_{fil_{max}}}\left(i_{L_{fil_{max}}}\right) \leq 0.8\, B_{sat}^{(MPP)} \tag{5.21}$$

$$n_L\, A_{wire} \leq k_F\, W_{A_L} \tag{5.22}$$

$$n_{L_{fil}} A_{wire} \leq k_F W_{A_{L_{fil}}} \tag{5.23}$$

$$i_{L_{max}} < 0.7 I_{DS_{max}} \tag{5.24}$$

In the equations above, $i_{L_{max}}$ and $i_{L_{fil_{max}}}$ stand for the maximal current through the inductors L and L_{fil}, evaluated as in (3.40) (Chapter 3). $B_{sat}^{(HFlux)} = 1.5T$ and $B_{sat}^{(MPP)} = 0.8T$ are the saturation flux density of the selected magnetic cores; the terms W_{A_L} and $W_{A_{L_{fil}}}$ refer to the core winding area available for the winding conductors, as indicated in Fig. 3.12, Chapter 3, which is extracted from the inductors spreadsheets in Fig. 5.4 and Fig. 5.5 through the inductor indexes In_L and $In_{L_{fil}}$. k_F is the filling factor which addresses the utilization ratio of the winding area W_A, assumed $k_F = 3$ in the performed routines. $I_{DS_{max}}$ is the maximal current rating of the specific switch, addressed through the MOSFET index In_{MOS}.

As for the stability aspect, a discrete modelling of the system is applied for an appropriate analysis of the cyclic behaviour of the system in steady-state.

A discrete time map of the state space vector of the controlled with a sampling period equal to the switching one (T_s) is built for each solution, as shown in Section 4.6.3. It has been shown that it is possible to obtain the Jacobian matrix of the closed loop system from the first order Taylor expansion of the system in (4.95). Following the same approach used in Section 4.6.3, the stability of each design solution is verified by evaluating the eigenvalues λ_i of the controlled system:

$$|\lambda_i| < 1, \qquad i = 1, \dots 5 \tag{5.25}$$

All the conditions showed in this section can be merged in a vector function and reconducted in the inequality form mentioned in (5.9):

$$\boldsymbol{h}_i(\boldsymbol{x}) < 0 \tag{5.26}$$

It is worth remarking that the input current ripple and output voltage excursion constraints are not included in the constraint function. The C_o and C_{fil} values are dependent variables automatically evaluated to fulfil these specifications for each element (genome) of the algorithm population, as explained in 5.2.1.

5.2.4 Optimization results

Fig. 5.9 shows the objective functions values of the Pareto solutions obtained with a gate resistance value set to $R_{gate} = 10\Omega$ and for an instantaneous load transient ($t_{LT} = 0$). The algorithm was performed in 118 iterations and 27 hours. Table 5.4 shows the range of the obtained values of the optimal solutions genes (independent variables), highlighting the direction of their variations with the increasing of the solution power losses value (ascending power losses, in Fig. 5.9). For example, the switching frequency f_s of the optimal solutions increase along with power losses $P_{(converter)}$, hence in the reverse sense of the volume value $V_{(converter)}$. Indeed, the decreasing of C_o and L volumes as f_s increases outweighs the increasing of the heatsink size. The increase of the L comes along with the increase of the respective core size (In_L) and of the number of turns n_L.

The value of the attenuation Att_{DM} ((3.75), Chapter 3) required by the input filter at the switching frequency reasonably grows in a opposite direction than the inductance value L, then along with the L current ripple value Δi_L, despite the increase of the switching frequency f_s. The most recurrent semiconductor device is the E3M0065090D of the CREE brand, indexed $In_{MOS} = 8$ in the spreadsheet

in Fig. 5.7. It indeed exhibits one of the lowest products values $r_{DS}(Q_{GD} + Q_{GS})$ product values, in the last column, which can be considered as a fitness value to address the trade-off between conduction and switching losses.

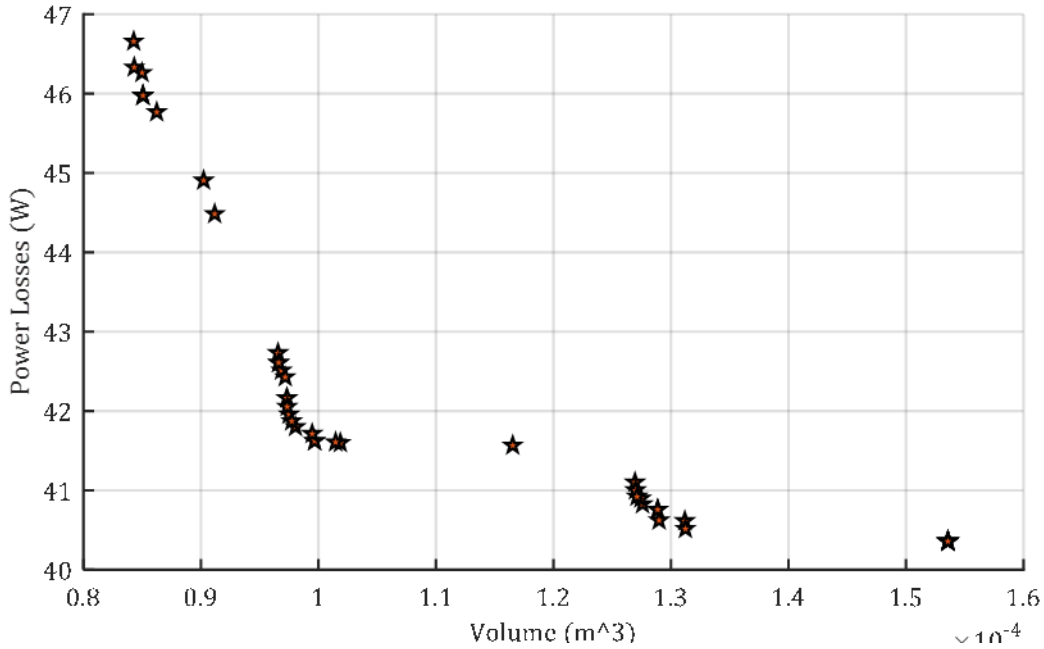


Fig. 5.9 Pareto Front of the optimization routine run with $R_{gate} = 10\Omega$, $t_{LT} = 0$ for the operating point described in Table 5.1.

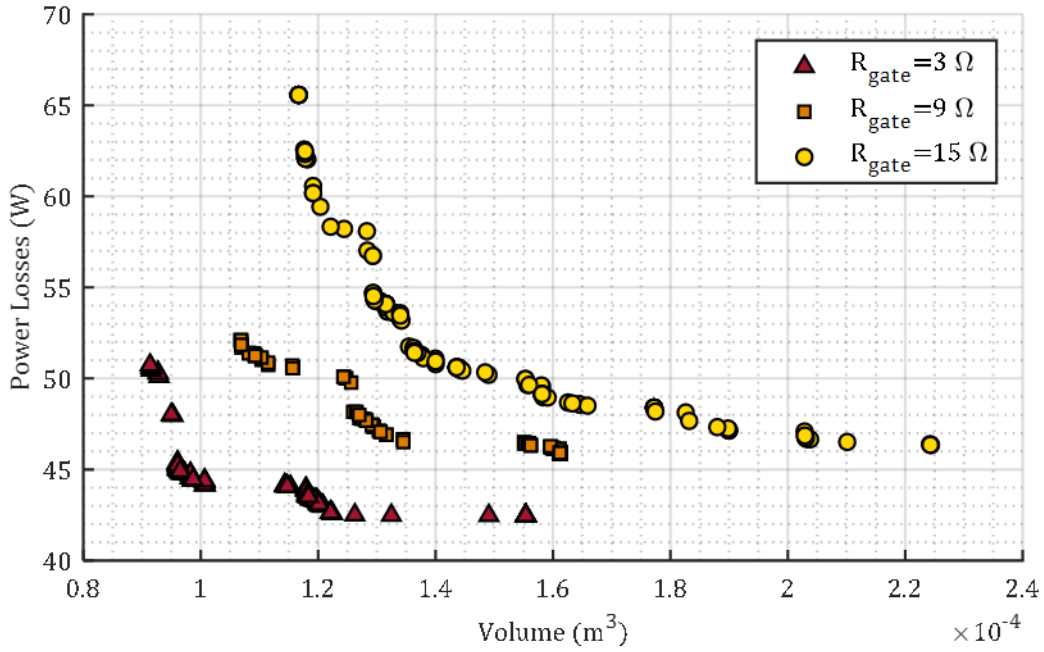
Table 5.4 Range of variation of the design variables for the optimal results in Fig. 5.9.

Variable description	Variable range in the ascending sense of the power losses
f_s	$30kHz \rightarrow 50kHz$
L	$460\mu H \rightarrow 160\mu H$
C_o	$75\mu F \rightarrow 35\mu$
Att_{DM}	$1.9 \rightarrow 4$

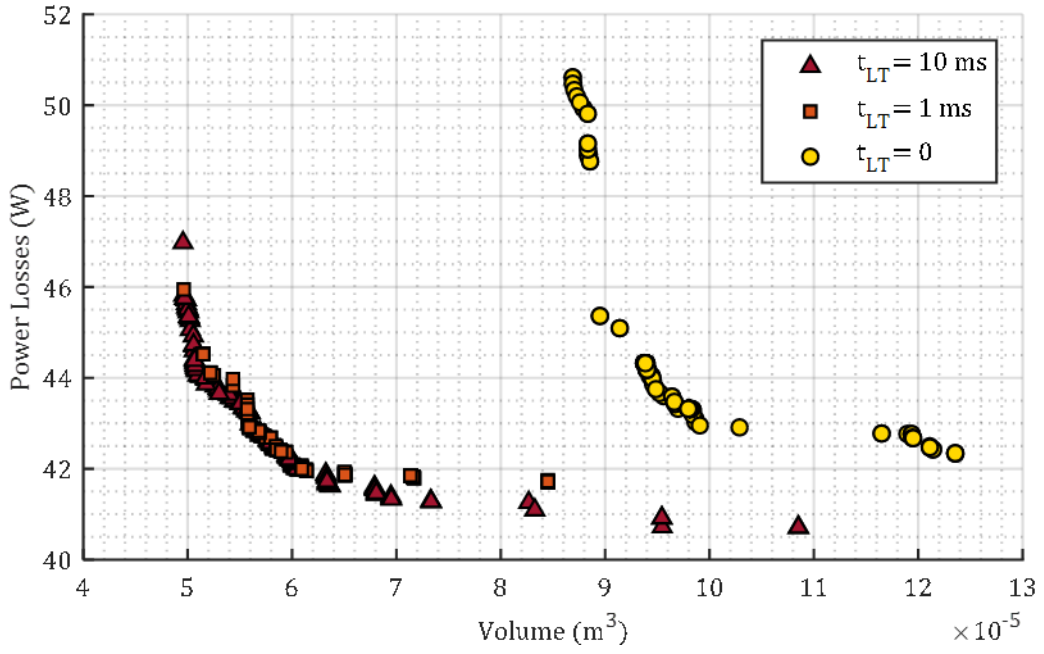
The Pareto Fronts depicted in Fig. 5.10(a) shows the optimization results obtained for different values of the gate resistance. Smaller the switching times, better the performances. As expected, diminishing the gate resistance R_{gate} implies faster commutation times, in turn the losses decrease and the heat sink is more compact. On the other hand, both current and voltage slope are steeper, resulting in greater harmonic content, hence a bulkier EMI filter.

In Fig. 5.10(b), the optimization is conducted for different transient times t_{LT} of the load power. As expected, steeper load variations require bulkier passive components in order to respect the design constraints; hence, the Pareto Front performed for $t_{LT} = 0$ appears transposed toward the right. The optimization results obtained for $t_{LT} = 1ms$ and $t_{LT} = 10ms$ have almost the same performances. Indeed, as soon as the $t_{LT} > 0$, the steady state constraint on the voltage excursion after a step-up or step-down load power become more restrictive than the transient state constraint.

In order to show the effectiveness of the constraint function, another optimization routine was performed, whose results are showed in Fig. 5.11. In this case, the stability check has been applied just to the optimal solutions in the Pareto Front (with a remarkable gain of time).



(a)



(b)

Fig. 5.10 Pareto solutions obtained for different values of the driver circuit gate resistances (a) (with $t_{LT} = 0$) and for different load transient periods t_{LT} (b) (with $R_{gate} = 4\Omega$)

Because of its built-in inductor L, the boost converter notoriously needs a low attenuation of the input current, consequently the $L_{fil}C_{fil}$ filter impedance does not usually provoke instability for the operating point considered in Table 5.1.

This is why in the aforementioned cases, even if the algorithm is performed without the constraint function on the stability, the whole set of the final optimal solutions are always stable. This is no longer true in the following case.

An optimization has been conducted for an application which requires a higher load power P_o (5kW instead of 3kW) and a more stringent attenuation of the input current Δi_{in} ($\Delta i_{i_{lim}} = 1\%\ I_i$, instead of $\Delta i_{i_{lim}} = 14\%\ I_i$). The gate resistance value has been set to $R_{gate} = 2\Omega$, in order to lead toward solutions with higher switching frequencies, then a higher controller bandwidth for (5.15). These three conditions push the algorithm to reach design solutions more likely to provoke unstable interaction between the output impedance of the input $L_{fil}C_{fil}$ filter and the input impedance of the converter $Z_{in}^{(cl)}$.

In order to highlight the instable solution (marked in red on Fig. 5.11), the stability criterion has only been applied to the solution of the Pareto front. This modification was also particularly beneficial in regards to the processing time (4h instead of 27h). Compared to Fig. 5.9 and Fig. 5.10, due to tighten constraints, the solutions are bulkier and exhibit higher power losses.

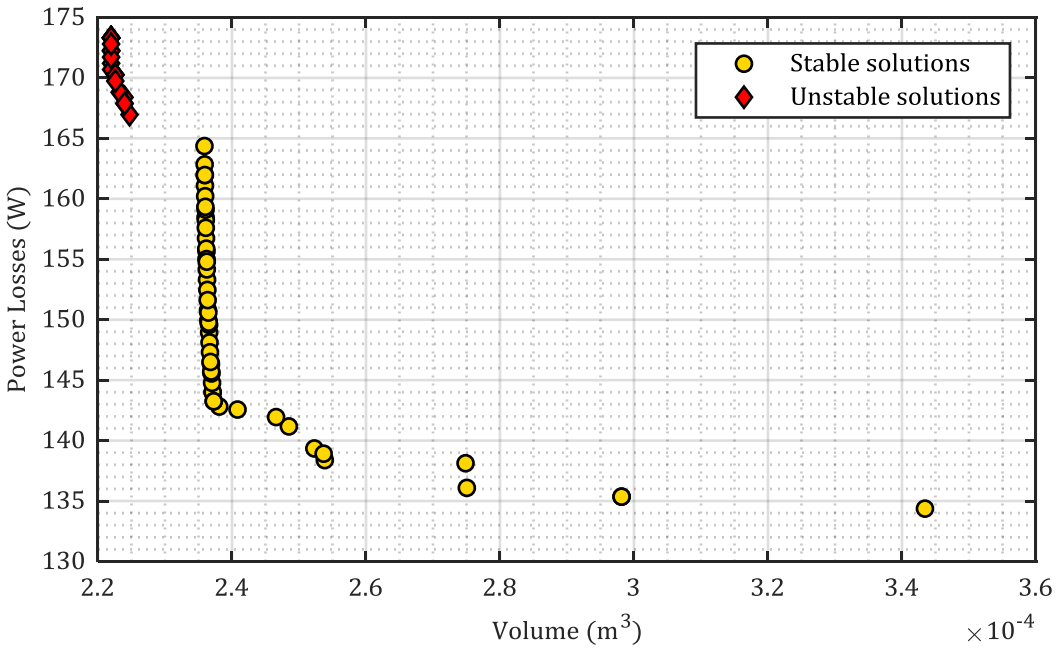


Fig. 5.11 Pareto Front results ($V_{in} = 270V$, $V_o = 350V$, $P_o = 5kW$, $t_{LT} = \infty$, $R_{gate} = 2\Omega$, $\Delta i_{i_{lim}} = 1\% I_{in}$).

5.3 Experimental results

A boost converter prototype has been realized and a test-bench has been set up to prove the validity of the study. There may be discrepancies between the parameters provided by the manufacturers and the actual components' parameters (for instance the non linear MOSFETs capacitances, the permeability of a magnet core, geometrical dimensions and so on). As a result, the experimental solutions could exhibit a slightly different behaviour than the theoretical one towards the performances (losses, current ripple and voltage ripple) and the expected constraints (stability, authorised ripple). For these reasons, the constraint function in the routine includes safety margins (for example current ratings, magnetic saturation or stability) to ensure the reliability of the implemented solutions. The main objective of the experimental bench is, indeed, to confirm the feasibility and reliability of the converter designed

according to the obtained optimal solutions, the losses model employed for the optimization procedures and the compliance with the design specifications in both steady-state and load transient conditions.

The circuital scheme in Fig. 5.12 depicts the main blocks of the experimental set-up. A TDK-Lambda GEN 300-17 supplies the boost converter input voltage. The power load consists of a cascaded converter. The current controlled step-down chopper emulates an ideal CPL ($L_{HB} = 600\mu H, R = 10\Omega$).

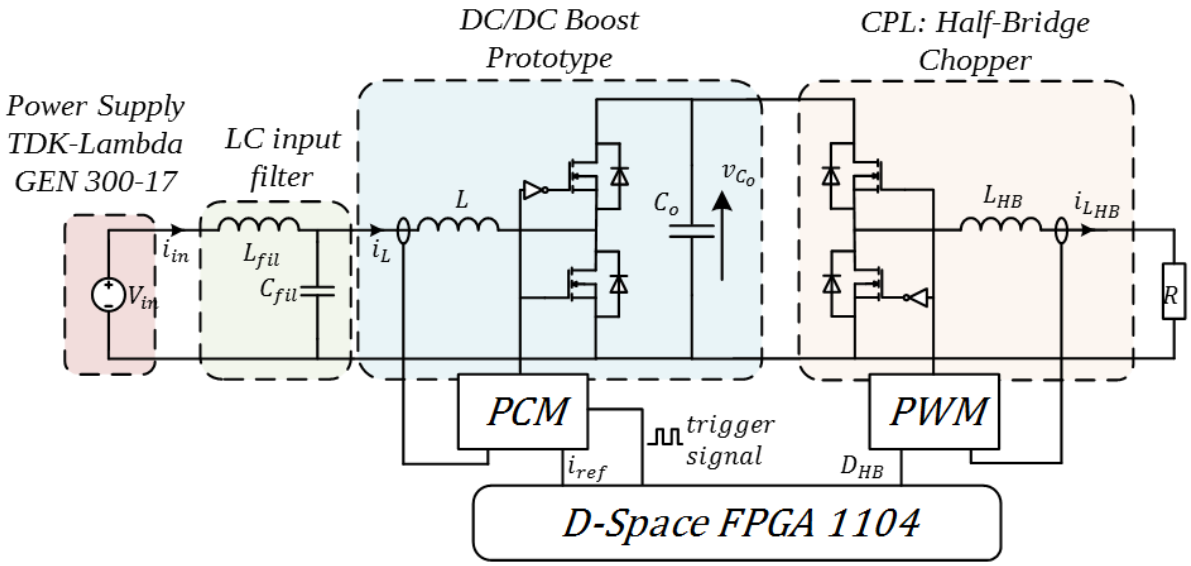


Fig. 5.12 Test bench scheme.

On the market, the available integrated circuits for the realization of the peak current controllers are always associated with an analogic network to compensate the current loop with a voltage mode outer controller. This function is not compatible with an energy control loop. Consequently, the peak current controller was designed at the laboratory, implemented on an electronic circuit and mounted on the power board.

The outer energy loop was implemented on MATLAB/Simulink and coded on a D-Space FPGA board, which provides a scaled signal for the reference i_{ref}, with a sampling period of T_s. Moreover, the FPGA Board provides the signal of the trigger signal of the peak current controller and the control input D_{HB} to the chopper converter.

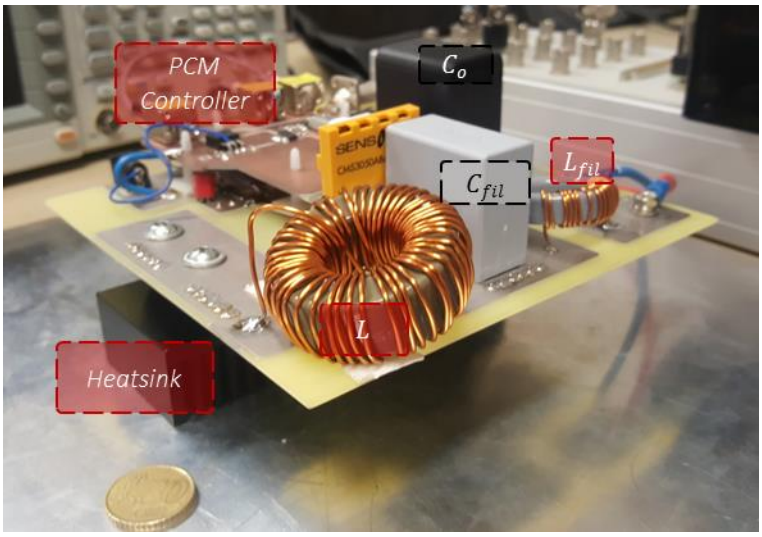
The power converter prototype, build according the design solution in Table 5.5 and components referenced in Table 5.6, is shown in Fig. 5.13(a).

The design solution described in Table 5.5 has been designed for the operating point and specifications described in Table 5.1 and validated on the experimental test bench for a 3kW instantaneous transient load ($t_{LT} = 0$).

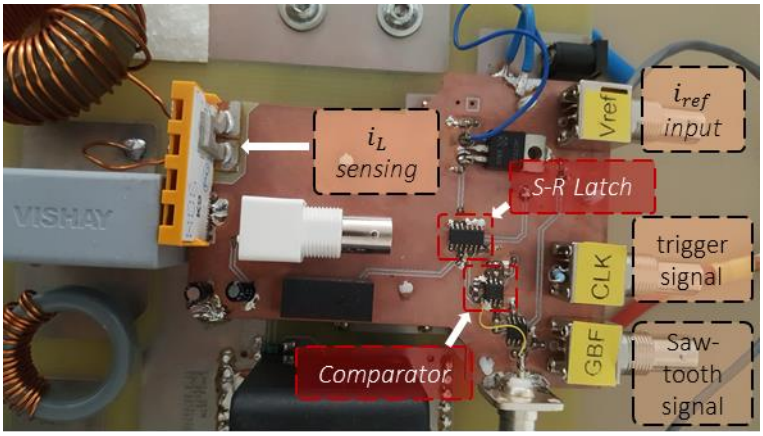
Due to the limitations and the inaccuracies of the current and voltage probes, measuring the power losses of a highly efficient converter can be pretty challenging. Consequently, the power has been monitored by a Yokogawa WT1800 Power Analyser showed in Fig. 5.14. The expected and obtained power losses and the volume are showed in Table 5.7.

The measured power losses value ($\eta_{(mesured)} = 98.5\%$) is consistent with the expected one ($\eta_{(evaluated)} = 98.4\%$), evaluated as in Section 5.2.2, which confirms the reliability of the power losses model employed. The heatsink size was adapted to the power module surface, as shown in Fig. 5.13, for this reason its volume results bigger than the needed one ($V_{(heatsink)}^{evaluated} = 20.5cm^3, V_{(heatsink)}^{real} = 88.5cm^3$). As an additional information, even if not an optimization target, the total mass of the converter is $m_{(converter)} = 600\ g$ (power module excluded).

The input current waveform in steady state is depicted in Fig. 5.15. As expected, the input current $i_{L_{fil}}$ respects the input ripple constraints at the nominal power $\Delta i_{L_{fil}} = 0.8A < \Delta i_{i_{lim}}$.



(a)



(b)

Fig. 5.13 Boost converter prototype with input filter (a) (components references in Table IV) and peak-current controller analogic circuit (b).

Table 5.5 Design solution employed for the realization if the experimental bench.

$\boldsymbol{x}$	Description	Value
$n_L, n_{L_{fil}}$	L, L_{fil} coils number	$46, 18$
$In_L, In_{L_{fil}}$	L, L_{fil} core indexes	$24, 21$
$In_{\mu_L}, In_{\mu_{L_{fil}}}$	L, L_{fil} permeability indexes	$5, 4$
f_s	Switching frequency	$20kHz$
i_{MOS}	MOS index	29

Table 5.6 References and description of the components employed for the experimental bench.

Reference	Description	Value
BSM08012P2C008	MOSFET	
	Switching freq.	$f_s = 20\ kHz$
MKP1848C67560JY	Output capacitor	$C_o = 100\mu F$
C058438A2	Main Inductor	$L = 436\mu H$
MKP1848C61560JP	Filter capacitor	$C_{fil} = 20\mu F$
C055586A2	Filter inductor	$L_{fil} = 15\mu H$
	Gate resistance	$R_{gate} = 4\Omega$
	Wire section	$A_{wire} = 0.79mm^2$

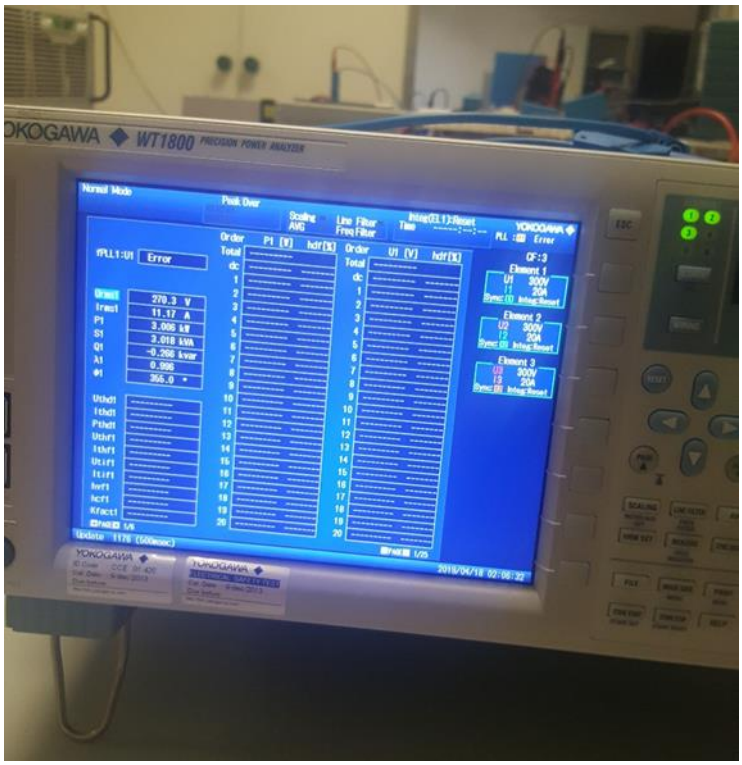


Fig. 5.14 Yokogawa WT1800 Power Analyser employed for the power losses measurement.

Table 5.7 Expected and real objective functions values of the selected design solution.

	Volume (cm3)	Power Losses (W)
Analytical	175	48
Experimental	242.8	46

Fig. 5.16 depicts the obtained waveforms during an instantaneous transient of the load power from $0kW$ to $3kW$. For the proper regulation of the controlled variable and the rejection of power load variations, the output power measure needs a particular attention.

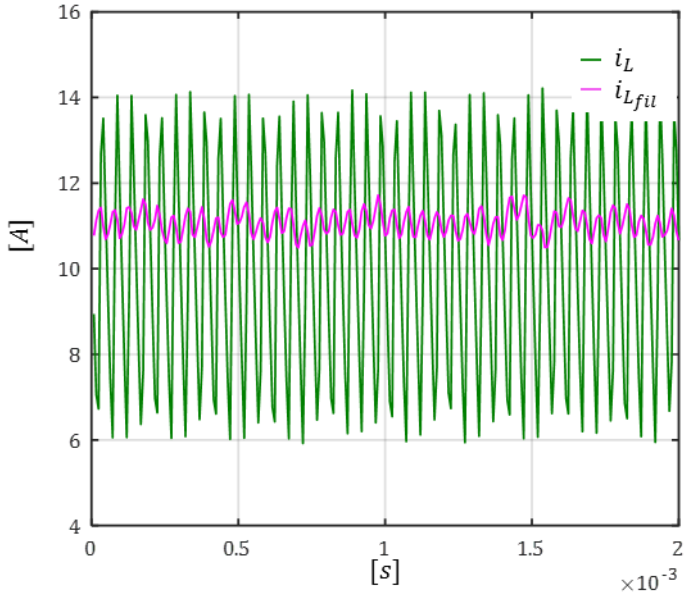


Fig. 5.15 Input current $i_{L_{fil}}$ and inductor current i_L waveforms in steady state.

As mentioned, the D-Space Board generates the current reference signal i_{ref} , evaluated as in (4.37), Chapter 3, for the inner peak current analogic controller. At the same time, it controls the cascaded converter through a Sliding controller, and generates the duty cycle D_{HB}. A PWM block transforms the load converter controller signal D_{HB} in the command inputs for the load converter switches. The output power P_o term is evaluated through the measure of the inductor current in the load converter $i_{L_{HB}}$:

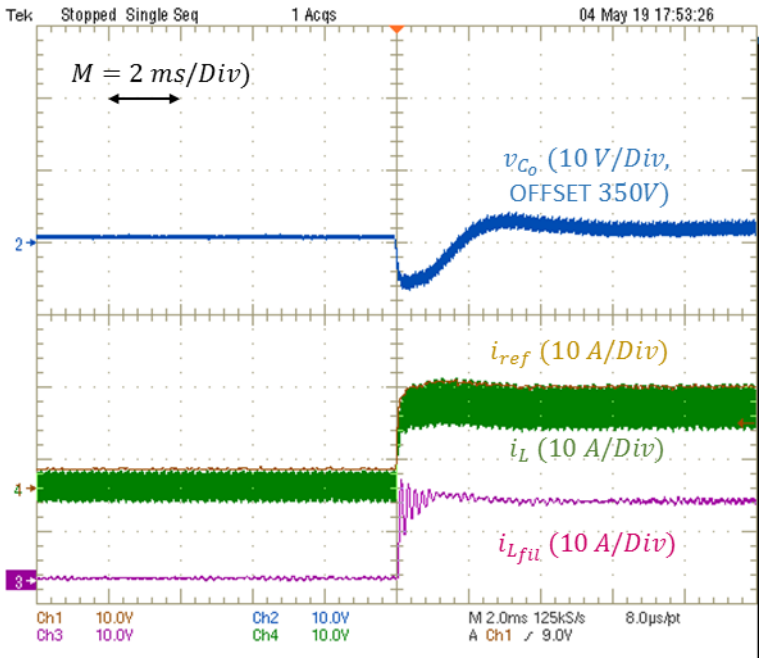
$$P_o = D_{HB}\, i_{L_{HB}} v_{C_o} \tag{5.27}$$

The measure of the output power is a sensitive issue. The expression in (5.27) represents the average value of the output power over the switching period T_s. The value $i_{L_{HB}}$ depends indeed from the sampling time, which means that, if not chosen opportunely, the measured $i_{L_{HB}}$ value could span in the range $[i_{L_{HB}} - \Delta i_{L_{HB}}/2,\, i_{L_{HB}} + \Delta i_{L_{HB}}/2]$. Furthermore, the active switches leg of the load converter is composed of an SKM 50GB123D IGBTs module, by Semikron, commanded by an SKHI22BH4R integrated driver, which is featured by an important dead time ($t_{dt} = 4\mu s$). Such imperfections are compensated by the integrator of the PI controller of the chopper load converter in steady state, but during fast transient it has a significant impact on the transient waveforms. The D_{HB} value has been corrected as in (1.7) so that the value of P_o provided to the energy controller (Fig. 4.14, Chapter 4) is consistent with the reality:

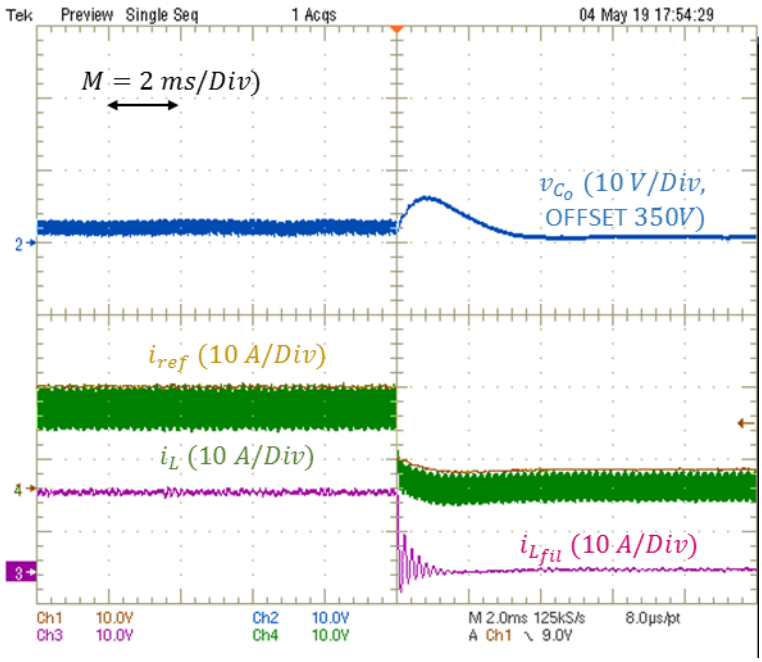
$$D'_{HB} = (D_{HB} + a_{HB}) b_{HB} \tag{5.28}$$

For the considered results the corrective factors have been tuned as $a_{HB} = -0.08$, $b_{HB} = 0.85$.

The v_{C_o} ripple amplitude in steady state $\Delta v_o^{(steady)} = 2.1V$ is far below the output voltage specification $\Delta v_{o\,lim} = 7V$, since the capacitance C_o has been designed for load transient case, as explained in Section 5.2.1. The variation of the output load power P_o provokes the step of the current reference i_{ref} ((4.37), Chapter 4). The energy controller parameters are evaluated as in (5.15), with $k_i = 1.5791 \times 10^6$ and $k_p = 1.7593 \times 10^3$. The inductor current i_L and the output voltage v_{C_o} follow their respective references. During the load transient events, since the filter state variables are not controlled, the input current rings at its resonance frequency, without leading to any instabilities.

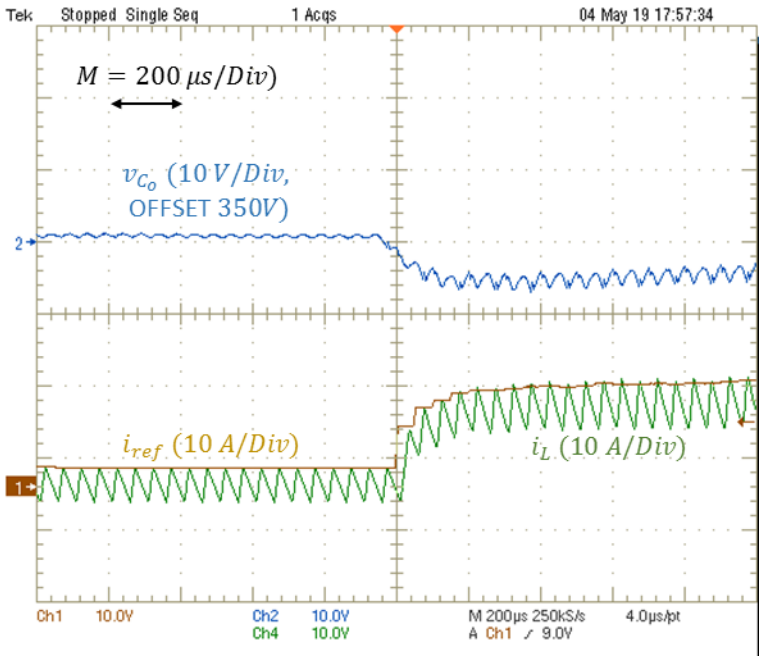


(a)

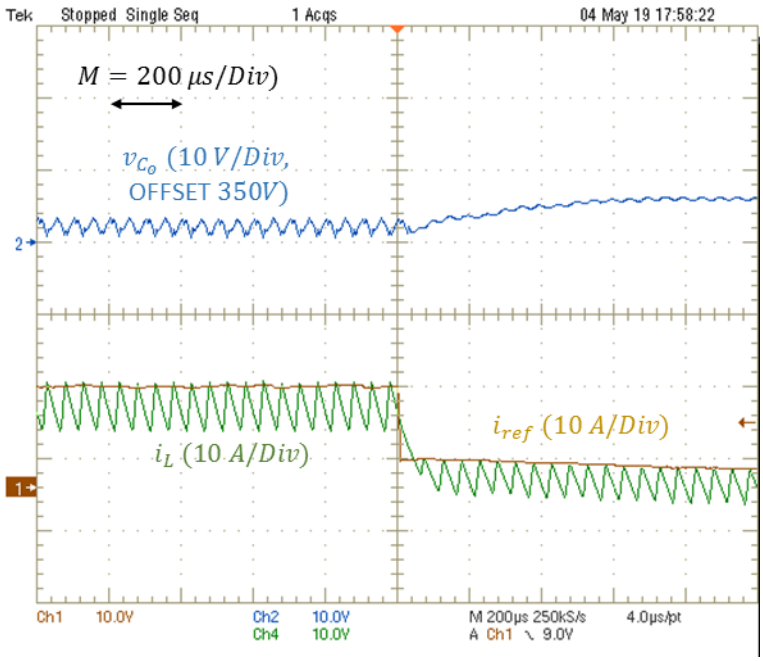


(b)

Fig. 5.16 Output voltage v_{C_o}, reference i_{ref}, inductors' currents i_L and $i_{L_{fil}}$ waveforms during the step-up (a) and step-down (b) load transients.



(a)



(b)

Fig. 5.17 Output voltage v_{C_o}, reference i_{ref}, inductors' currents i_L and $i_{L_{fil}}$ waveforms during the step-up (a) and step-down (b) load transients, zoomed.

The experimental waveforms exhibits some discrepancies with the theoretical ones, because of the non-ideal dynamical behaviour of the load converter and the practical limitations of the controller, such as the sampling effect and the computing step of the FPGA board. The first problem concerns the realization of a power load applying the desired load power steps. As mentioned, the load consists of a cascaded step-down chopper converter. The variation of the power delivered by the boost converter depends strictly on the dynamic of the load converter. For this reason, the power step has a variation profile smoother than the expected one, as it is possible to observe through the i_{ref} evolution in Fig. 5.16. This should lead toward a lower undershoot of the output voltage. On the other hand, this benefit is counterbalanced by the non-ideal behaviour of the controller. The D-Space FPGA board elaborates

the reference with a sampling time equal to the converter switching period T_s. The reference value is updated after a computation step of a sampling period. The power variation of the P_o term in the control law is visible just after a delay of T_s. It means that the output capacitor C_o starts providing on its own the current to the load a period T_s before that the controller react to the load power variation.

The output voltage waveform complies with the design forecast and it stays within the required limits ($\Delta v_{C_o} = 7\ V = \Delta v_{o_{lim}}$). The experimental results presented here confirm the validity of the proposed optimization procedure, which fulfil the voltage specifications both in steady-state and during the load transients.

5.4 Conclusions

In this chapter, the limits of traditional design approaches for power converters has been discussed, especially when multiple performances optimization are required. The most employed tools for the resolution of a multi-objective optimization problem in the domain of the power conversion consist in stochastic algorithms, based on evolutionary concepts. Namely, the fundamentals of a multi-objective problem have been properly introduced, and the resolution approach based on an elitist genetic algorithm has been discussed. More specifically, a non-dominated genetic algorithm has been employed, which guarantees both convergence and diversity of the design solutions. After a brief introduction of the NSGA II structure and main steps, the design problem of the system composed of a 3kW DC-DC boost converter and the differential input filter has been properly formulated in order to fit with the optimization procedure. Hence, the objective and the constraints functions have been defined according to the converter components' models described in the manuscript. The considered design variables have been opportunely chosen according to the degree of freedoms of the problem and in order to address the commercial availability of the converter components. The design specifications include the excursion limit of the output voltage both in steady state and during load transient events, and the DO-160 requirements at low frequencies on the input current ripple in steady state. The converter supplies a CPL, which represents the most unfavourable case in terms of stability. In literature, the proposed converters optimizations aim to develop design procedures only for the steady-state operating mode; the dynamic behaviour in case of disturbances or variations of the operating point is often neglected in the design phase. In the proposed method, since the converter is designed to withstand possible load power transients, the control strategy and its parameters have been included in the optimization routine. Moreover, due to the presence of the input LC filter, the optimization algorithm includes the study of the system stability by means of limit cycles and discards the unstable design solutions. The algorithm finds the optimal design solutions, which are the best trade-off between volume and power losses. The obtained solutions have been analysed in order to highlight the optimal values of design variables and the resulting trade-off. The Pareto fronts obtained by the genetic algorithm show that it is possible to increase the converter performances by a proper choice of the transistors drivers' parameters. Furthermore, the evaluated results show how the transient profile of the demanded power affects the volume of the optimal design solutions. In order to demonstrate the stability of the system, the feasibility of the design solutions and the compliance with the specifications and the expected losses value, a high efficiency converter corresponding to one of the designed solutions has been set. The experimental tests confirm the compliance with all the requirements, and consequently validate the effectiveness of the proposed optimization procedure.

General Conclusions

In the presented work the design problem of a DC/DC converter has been discussed. In Chapter 1, it has been shown that in embedded applications, such as electric vehicles or modern aircrafts, several loads on-board require a DC voltage supply. The electric energy distribution is provided through one DC voltage bus at least. The DC/DC conversion on-board is widely employed to adapt the several loads to the DC bus. In the particular case of the modern aircrafts, several pneumatic and mechanical parts have been replaced by electric actuators for the sake of weight and efficiency. In the More Electric Aircrafts, the mechanical gearbox unit for the generation of electric energy from the gas turbine has been suppressed, which leads to the generation of an AC voltage with variable frequency and variable magnitude. Then voltage of the DC micro grid is obtained by rectifying the AC voltage, then it can exhibit a large variation from its nominal value. Then, the power loads connected on the DC bus need to be adapted through a DC/DC converter.

The DC/DC conversion occurs through the use of switched mode power supplies (SMPS), whose operation take place thanks to switching transistors. As explained in Chapter 1, the wide band-gap semiconductor based transistors are mature enough to replace the IGBTs in the low/medium voltage range and for power values up to 100kW. Materials such as the Silicon Carbide allow to build unipolar devices, like MOSFETs, able to reach higher switching frequencies and fewer power losses, which offer the possibility to remarkably improve compactness and efficiency of the power converters. These features are particularly required for embedded applications to ensure the longest autonomy.

This study focuses on the power electronics that supply an actuator in an embedded environment such as an aircraft or an electric/hybrid vehicle. The weight and the efficiency of the actuation chain, composed of an inverting block and the motor, can be indeed optimized if a DC/DC converter is inserted between the DC bus and the inverter. The most common topologies have been listed in Chapter 2. Moreover, a new topology, partially based on the Quasi Z architecture, have been proposed for a wide speed range mission profile. This topology owns step-up/down function and a continuous input current, whose ripple can be even suppressed through an opportune coupling of the magnetic components. This feature allows to reduce the size of the input filter or even remove it. The input filter is indeed necessary to uniform the current and voltage harmonics conducted to the network as stated in the application standards (DO-160F for the considered case). The proposed topology has been compared with a SEPIC converter (which has common features, such us step up/down non-inverting voltage gain, with continuous input current and possibility to suppress the input current ripple) in terms of stress on the components and energy stored by the passive elements. The results reveal that in the considered voltage gain range [0.5,1.5], the proposed topology exhibits lower current/voltage stresses on the active components and lower stored energy, which leads to the choice of smaller passive components.

Nevertheless, as dealt in Chapter 3, the design of a DC/DC converter is not a trivial task, especially when the objective consists of optimizing two performances, such as volume and power losses. A DC/DC boost converter has been chosen in this work to provide a design procedure example. The operating principles and the properties of the several parts of the converter have been described, as well as the relative power losses models (with a particular focus on the active components) and the factors that determine their size. All the aspects to be considered in the design of the magnetic components, capacitors, switching devices and cooling unit were discussed. It has been highlighted how much the choice of each parameter relative to the design of any component impacts directly or not on the others. Especially when the design objectives are more than one, trade-offs are inevitable. The choice of the active components determines the most of the power losses of the converter, the reachable switching frequency and the size of the cooling unit. The design of the passive components (of both converter and

input filter) is strictly related to the switching frequency, as well as the operating point and the current and voltage ripples specifications. In Chapter 3, the passive components have been designed for the only steady state operation. When the mission cycle includes variations of the operating point, the passive components impact on the voltage and current variation during the transient time, along with the control strategy and its rapidity. If not properly designed, the converter may not comply with the design specifications during the transient state, or even compromise the reliability of the converter. For the considered application, it has been shown in Chapter 4 that an excessive variation of the load current (as consequence of a fast variation of the mechanical torque), may provoke a large excursion of the converter output voltage, then the inverter input voltage, and impact on the controllability of the motor phases currents. In order to find an optimal design solution, the design procedure of the power stage cannot be carried out separately from the controller one. For the case under study, the control strategy has been chosen specifically for the rejection of the power load variations. Subsequently, an analytical relationship was established to relate the output voltage undershoot and overshoot, the power stage and the controller parameters in case of a transient of the load power. Such relation is useful to design the passive components inductance and capacitance values in order to satisfy the output voltage specifications in transient state, which is usually more binding than the steady one. Once the control strategy and the controller parameters have been defined, the closed loop system stability can be ensured as well, especially when an input filter is required for the input current harmonics to meet the standards imposed by the application. In fact, the interaction between two cascaded stable subsystems, as in the case of the input filter and the converter, can lead to instability, especially if the resonance frequency of the filter lies within the gain bandwidth of the closed loop system. To analyse the stability of the system over a wide frequency range, the closed loop system extended to the input filter was mapped in the discrete domain (Chapter 4), since the average model analysis is no longer appropriate.

While optimising the compactness and efficiency of the converter's power circuit alone was a non-trivial task, it is even more complicated if the dynamic behaviour is taken into account, including the control strategy and the respective parameters. An analytical solution of such problem is not possible, because of its complexity (several relations are in a non-explicit form) and because it does not exist a unique solution which ensures the optimality of both volume and power losses. For such reasons, an evolutionary algorithm has been preferred. In Chapter 5, a multi-objective genetic algorithm, namely the NSGA-II, has been employed. The procedure lead to a Pareto Front, i.e. a series of the most convenient design solutions. Furthermore, the algorithm takes into account the active and passive components availability on the market.

One of the obtained solutions have been realized and tested experimentally in Chapter 5. The prototype of the boost converter shows a good agreement with the expected results in both steady and transient states. The controlled system is stable and the waveforms show compliance with the voltage and current specifications during a variation of the load power. Moreover, the measured power losses confirm the power losses model adopted.

This work should be considered as a basis for further developments in the future. In the following, several developments and alternative solutions are proposed:

- more converter topologies (the interleaved topologies represent an interesting path to explore) or controller strategies shall be investigated;
- the objective functions of the algorithm (volume and power losses) can be chosen differently, as for example the mass of the system or its reliability;
- The technology and the material of the components can be chosen differently. For instance, planar inductors have not been considered. More advanced and compact cooling units are available on the market, or different magnetic materials;
- The high frequency behaviour of the converter shall be included: the conducted emissions in the high frequency range is a pressing issue nowadays, especially when dealing with fast devices like the WBG ones. The high frequency behaviour requires an intensive study, which involves the high frequency profile of each component and the board layout. The complexity of this issue

makes it difficult to include it in a genetic algorithm, for this reason, in the manuscript, the switching times of semiconductor devices (or the gate resistance in this case) were treated as design parameters to be set in advance. A black box approach can be used to characterize the converter at high frequencies, as in [155].

- The components parameters provided by the manufacturers may not match with the actual ones. The discrepancies between the parameters provided by the manufacturers and the actual device can actually affect the performances of the converter. They are indeed provided within a confidence interval. In literature, two main approaches are developed to deal with a robust multiobjective optimization problem [156], [157]. The first approach aims to reduce the sensitivity of the solutions from the variation of the design parameters or variables, by searching for robust optimal solutions which achieves the best trade-off between optimization and robustness. In [158], a robustness performance model is defined and incorporated in the optimization. That means that the variance of the objective functions are considered along with the expected objective values. Another approach consists into defining and characterizing each solution with a *robustness index*, in order to help the designer to choose the most reliable solutions between the optimal ones [159]. The inclusion of the sensitivity study in the optimization procedure could be an interesting improvement of the presented work.

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Abstract:

Optimization of DC/DC converters for embedded systems including dynamic constraints

To keep up with the new emission standards and improve efficiency and autonomy, the transportation sector has moved towards more electric solutions. Then, compactness, weight and efficiency are primary requirements in modern aircrafts or Electric/Hybrid vehicles. The power electronics units in the on-board electrical networks have to be designed accordingly, as it is essential to achieve very compact designs and energy conversion efficiencies very close to the unity. The wide bandgap semiconductor materials are considered as the future technology in the realization of high efficiency switched-mode power supplies. Such materials are featured by fast switching behaviour and low power losses, which allows reducing the size of the passive elements and the cooling unit of the power converter. Considering these criteria, the objective of this study concerns the development of a procedure for the optimal design of a DC/DC boost converter 350V/3kW. The converter has been designed specifically for a powertrain application. In order to ensure the proper interaction with the load (DC/AC inverter and motor) and the micro-grid on-board, the design must take into account the stability and dynamic behaviour of the converter during a possible variation of the operating point, then its control strategy. To deal with the manifold technical solutions and in order to reach the best trade-off, a Pareto front genetic approach is proposed. The developed routine consent to obtain the most convenient design solutions in terms of efficiency and compactness, which ensure the stability and the compliance with the design specification on both steady state and transients modes.

Keywords: DC-DC Power Converters, Multi-objective optimization, Load Transient Response, Stability

Résume :

Optimisation des convertisseurs DC/DC pour systèmes embarqués avec prise en compte du comportement dynamique

Pour se conformer aux nouvelles normes d'émission et améliorer l'efficacité et l'autonomie des véhicules, le secteur des transports s'est tourné vers des solutions plus électriques. La compacité, le poids et l'efficacité sont alors des exigences primordiales dans les avions modernes ou dans les véhicules électriques/hybrides. Dès lors, la conception des éléments de conversion de puissance électrique demande un grand soin. Il est essentiel de proposer les solutions les plus compactes possibles et présentant les hauts rendements de conversion. Dans ce contexte, les matériaux semi-conducteurs à large bande interdite sont désormais reconnus comme étant les candidats les plus appropriés. En effet, ceux-ci se caractérisent par un comportement en commutation des plus rapide et par des pertes de puissance plus faibles (commutation et conduction), ce qui permet de réduire la taille des éléments passifs et de l'unité de refroidissement du convertisseur de puissance. Compte tenu de ces critères, cette étude a pour objectif le développement d'une procédure pour le dimensionnement optimale d'un convertisseur élévateur DC/DC350V/3kW. Le convertisseur a été conçu spécifiquement pour une structure d'alimentation d'un actionneur. Afin d'assurer la bonne interaction entre la charge (onduleur DC/AC et moteur) et le micro-réseau de bord, le dimensionnement doit prendre en compte la stabilité et le comportement dynamique du convertisseur lors d'une éventuelle variation du point de fonctionnement, donc sa stratégie de contrôle. Les alternatives technologiques à un tel problème sont multiples. Une sélection par algorithme génétique avec front de Pareto est proposée. La routine développée permet d'identifier les solutions à plus hauts rendement et compacité, tout en préservant la stabilité et le respect des spécifications, aussi bien en régime permanent que transitoire.

Mots Clés : Convertisseurs de puissance DC-DC, Optimisation multi-objectifs, Réponse aux transitoires de charge, Stabilité